

## Advanced PMU for Samsung S5PC100, S5PC110 and S5PV210 Processors

### FEATURES

- Optimized for Samsung S5PC100, S5PC110 and S5PV210 Processors
- Three Step-Down DC/DC Converters
- Four Low-Dropout Linear Regulators
- Integrated *ActivePath™* Charger
- I<sup>2</sup>C™ Serial Interface
- Advanced Enable/Disable Sequencing Controller
- Minimal External Components
- Tiny 5x5mm TQFN55-40 Package
  - 0.75mm Package Height
  - Pb-Free and RoHS Compliant

### GENERAL DESCRIPTION

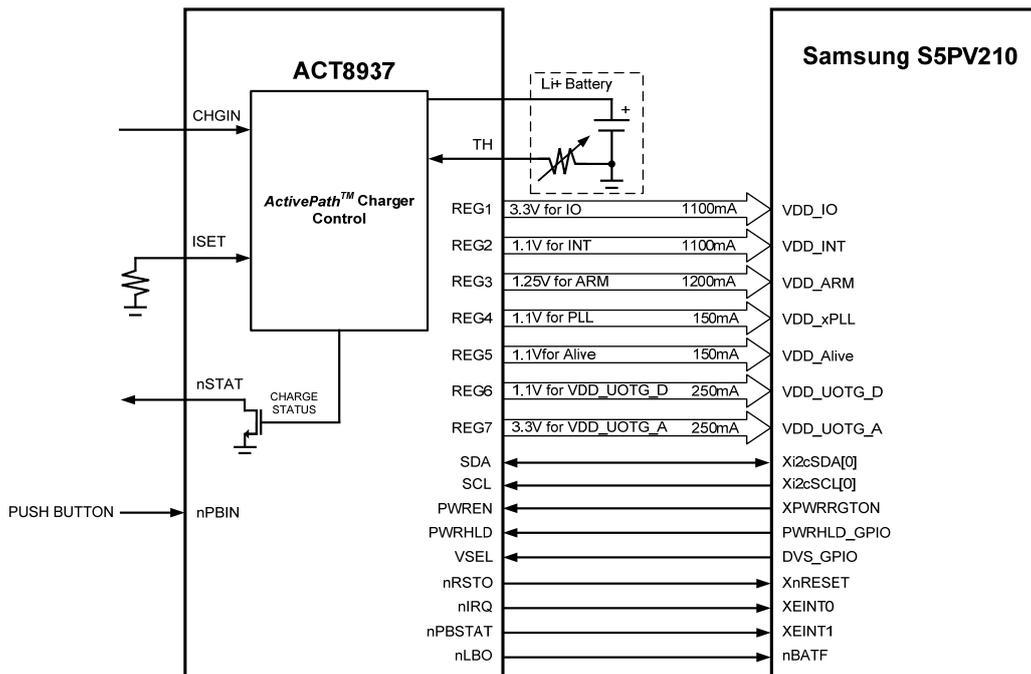
The ACT8937 is a complete, cost effective, highly-efficient *ActivePMU™* power management solution, optimized for the unique power, voltage-sequencing, and control requirements of the Samsung S5PC100, S5PC110 and S5PV210 processors.

This device features three step-down DC/DC converters and four low-noise, low-dropout linear regulators, along with a complete battery charging solution featuring the advanced *ActivePath™* system-power selection function.

The three DC/DC converters utilize a high-efficiency, fixed-frequency (2MHz), current-mode PWM control architecture that requires a minimum number of external components. Two DC/DCs are capable of supplying up to 1100mA of output current, while the third supports up to 1200mA. All four low-dropout linear regulators are high-performance, low-noise regulators that supply up to 150mA, 150mA, 250mA, and 250mA, respectively.

The ACT8937 is available in a compact, Pb-Free and RoHS-compliant TQFN55-40 package.

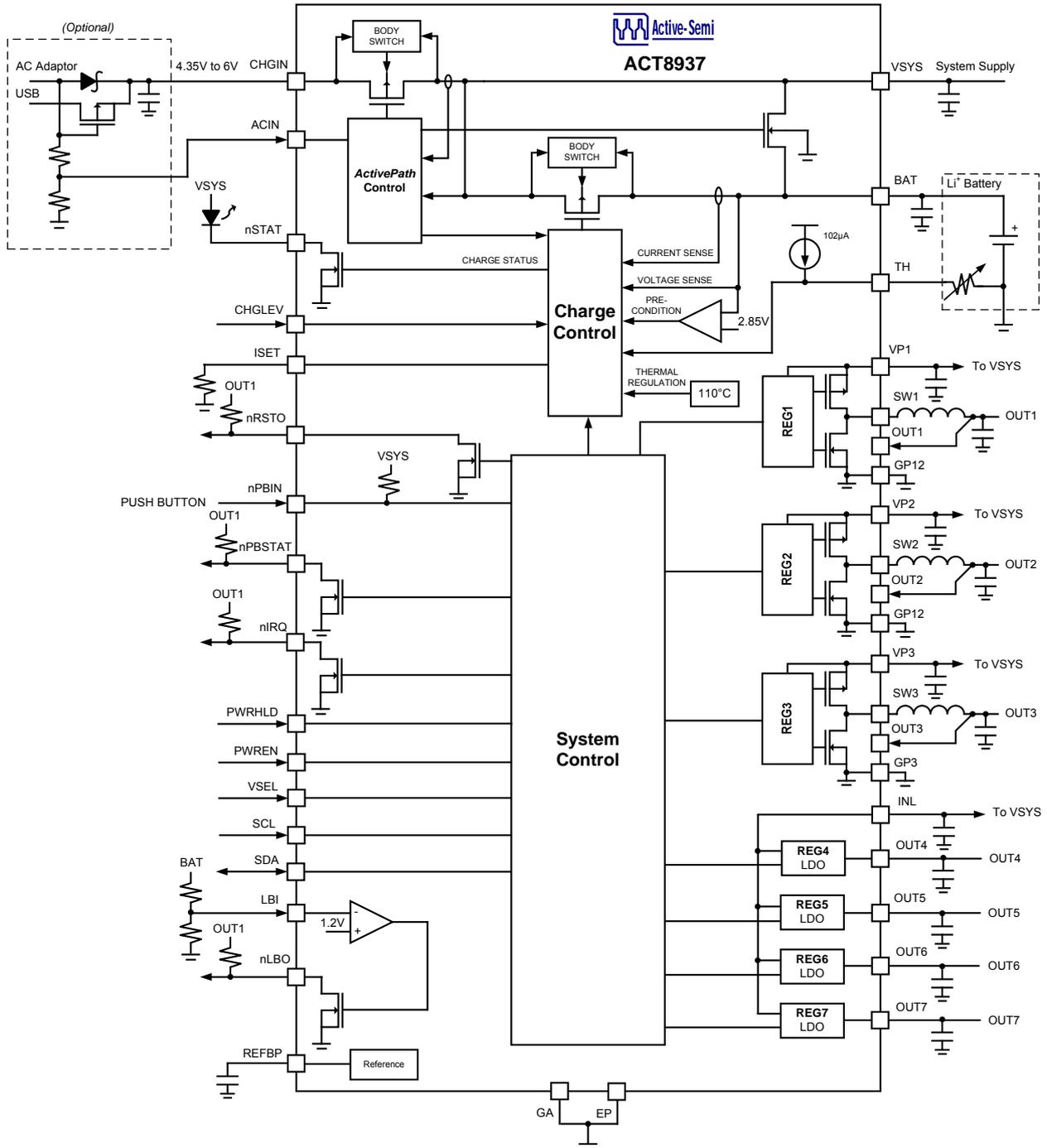
### TYPICAL APPLICATION DIAGRAM



## TABLE OF CONTENTS

|  |       |
|--|-------|
| General Information .....  | p. 01 |
| Functional Block Diagram .....   | p. 03 |
| Ordering Information .....   | p. 04 |
| Pin Configuration .....  | p. 04 |
| Pin Descriptions .....   | p. 05 |
| Absolute Maximum Ratings .....   | p. 07 |
| I <sup>2</sup> C Interface Electrical Characteristics .....              | p. 08 |
| Global Register Map .....  | p. 09 |
| Register and Bit Descriptions .....                                      | p. 10 |
| System Control Electrical Characteristics .....                          | p. 15 |
| Step-Down DC/DC Electrical Characteristics .....                         | p. 16 |
| Low-Noise LDO Electrical Characteristics .....                           | p. 17 |
| <i>ActivePath</i> <sup>TM</sup> Charger Electrical Characteristics ..... | p. 18 |
| Typical Performance Characteristics .....                                | p. 20 |
| System control information .....   | p. 27 |
| Interfacing with the Samsung S5PV210 .....                               | p. 27 |
| Control Signals .....  | p. 28 |
| Push-Button Control .....  | p. 29 |
| Control Sequences .....  | p. 29 |
| Functional Description .....   | p. 32 |
| I <sup>2</sup> C Interface .....   | p. 32 |
| Voltage Monitor and Interrupt .....                                      | p. 32 |
| Thermal Shutdown .....   | p. 33 |
| Step-Down DC/DC Regulators .....   | p. 34 |
| General Description .....  | p. 34 |
| 100% Duty Cycle Operation .....  | p. 34 |
| Synchronous Rectification .....  | p. 34 |
| Soft-Start .....   | p. 34 |
| Compensation .....   | p. 34 |
| Configuration Options .....  | p. 34 |
| OK[ ] and Output Fault Interrupt .....                                   | p. 35 |
| PCB Layout Considerations .....  | p. 35 |
| Low-Noise, Low-Dropout Linear Regulators .....                           | p. 36 |
| General Description .....  | p. 36 |
| Output Current Limit .....   | p. 36 |
| Compensation .....   | p. 36 |
| Configuration Options .....  | p. 36 |
| OK[ ] and Output Fault Interrupt .....                                   | p. 36 |
| PCB Layout Considerations .....  | p. 36 |
| <i>ActivePath</i> <sup>TM</sup> Charger .....                            | p. 38 |
| General Description .....  | p. 38 |
| <i>ActivePath</i> Architecture .....                                     | p. 38 |
| System Configuration Optimization .....                                  | p. 38 |
| Input Protection .....   | p. 38 |
| Battery Management .....   | p. 38 |
| Charge Current Programming .....   | p. 39 |
| Charger Input Interrupts .....   | p. 39 |
| Charge-Control State Machine .....                                       | p. 41 |
| State Machine Interrupts .....   | p. 41 |
| Thermal Regulation .....   | p. 42 |
| Charge Safety Timers .....   | p. 42 |
| Charger Timer Interrupts .....   | p. 42 |
| Charge Status Indicator .....  | p. 42 |
| Reverse-Current Protection .....   | p. 42 |
| Battery Temperature Monitoring .....                                     | p. 42 |
| Battery Temperature Interrupts .....                                     | p. 43 |
| TQFN55-40 Package Outline and Dimensions .....                           | p. 44 |

FUNCTIONAL BLOCK DIAGRAM



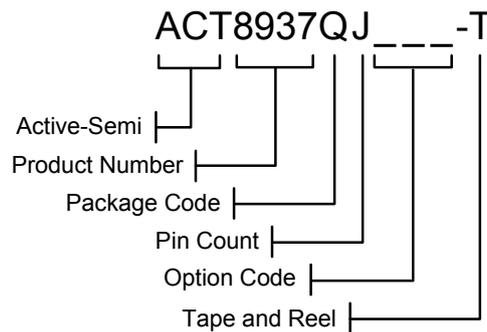
## ORDERING INFORMATION<sup>①②</sup>

| PART NUMBER    | V <sub>OUT1</sub> | V <sub>OUT2</sub> /V <sub>STBY2</sub> <sup>③</sup> | V <sub>OUT3</sub> /V <sub>STBY3</sub> | V <sub>OUT4</sub> | V <sub>OUT5</sub> | V <sub>OUT6</sub> | V <sub>OUT7</sub> | PROCESSOR          |
|----------------|-------------------|--|---------------------------------------|-------------------|-------------------|-------------------|-------------------|--------------------|
| ACT8937QJ1PQ-T | 3.3V              | 1.3V/1.2V  | 1.35V/1.2V                            | 1.2V              | 1.2V              | 1.2V              | 3.3V              | S5PC100            |
| ACT8937QJ11C-T | 3.3V              | 1.1V/1.1V  | 1.25V/1.25V                           | 1.1V              | 1.1V              | 1.1V              | 3.3V              | S5PC110<br>S5PV210 |
| ACT8937QJ106-T | 1.8V              | 1.1V/1.1V  | 1.25V/1.25V                           | 1.1V              | 1.1V              | 1.1V              | 3.3V              | S5PC110<br>S5PV210 |
| ACT8937QJ2PQ-T | 3.3V              | 1.3V/1.2V  | 1.35V/1.2V                            | 1.2V              | 1.2V              | 1.2V              | 3.3V              | S5PC100            |
| ACT8937QJ21C-T | 3.3V              | 1.1V/1.1V  | 1.25V/1.25V                           | 1.1V              | 1.1V              | 1.1V              | 3.3V              | S5PC110<br>S5PV210 |
| ACT8937QJ206-T | 1.8V              | 1.1V/1.1V  | 1.25V/1.25V                           | 1.1V              | 1.1V              | 1.1V              | 3.3V              | S5PC110<br>S5PV210 |

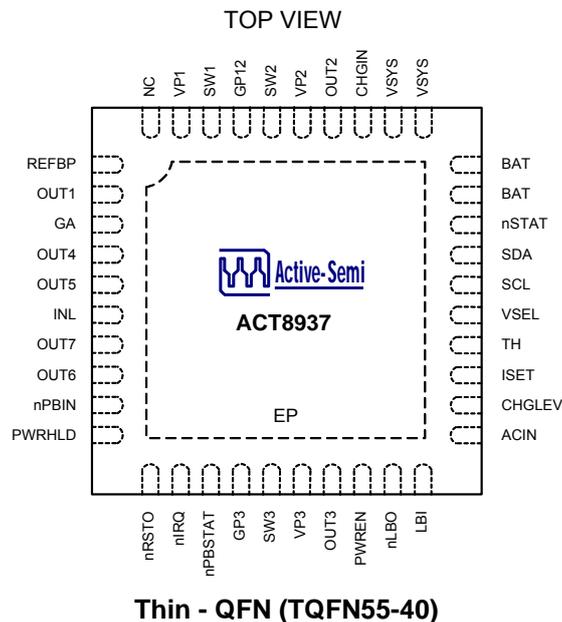
①: All Active-Semi components are RoHS Compliant and with Pb-free plating unless otherwise specified.

②: Standard product options are listed in this table. Contact factory for custom options. Minimum order quantity is 12,000 units.

③: To select V<sub>STBYx</sub> as the output regulation voltage for REG<sub>x</sub>, drive VSEL to logic high. V<sub>STBYx</sub> can be set by software via I<sup>2</sup>C interface. Refer to appropriate sections of this datasheet for V<sub>STBYx</sub> setting.



## PIN CONFIGURATION



## PIN DESCRIPTIONS

| PIN | NAME    | DESCRIPTION   |
|-----|---------|---|
| 1   | REFBP   | Reference Bypass. Connect a 0.047 $\mu$ F ceramic capacitor from REFBP to GA. This pin is discharged to GA in shutdown.   |
| 2   | OUT1    | Output Feedback Sense for REG1.   |
| 3   | GA      | Analog Ground. Connect GA directly to a quiet ground node. Connect GA, GP12 and GP3 together at a single point as close to the IC as possible.  |
| 4   | OUT4    | REG4 output. Capable of delivering up to 150mA of output current. Connect a 1.5 $\mu$ F ceramic capacitor from OUT4 to GA. The output is discharged to GA with 1.5k $\Omega$ resistor when disabled.  |
| 5   | OUT5    | REG5 output. Capable of delivering up to 150mA of output current. Connect a 1.5 $\mu$ F ceramic capacitor from OUT5 to GA. The output is discharged to GA with 1.5k $\Omega$ resistor when disabled.  |
| 6   | INL     | Power Input for REG4, REG5, REG6, and REG7. Bypass to GA with a high quality ceramic capacitor placed as close to the IC as possible.   |
| 7   | OUT7    | REG7 output. Capable of delivering up to 250mA of output current. Connect a 2.2 $\mu$ F ceramic capacitor from OUT7 to GA. The output is discharged to GA with 1.5k $\Omega$ resistor when disabled.  |
| 8   | OUT6    | REG6 output. Capable of delivering up to 250mA of output current. Connect a 2.2 $\mu$ F ceramic capacitor from OUT6 to GA. The output is discharged to GA with 1.5k $\Omega$ resistor when disabled.  |
| 9   | nPBIN   | Master Enable Input. Drive nPBIN to GA through a 50k $\Omega$ resistor to enable the IC, drive nPBIN directly to GA to assert a manual reset condition. Refer to the <i>nPBIN Multi-Function Input</i> section for more information. nPBIN is internally pulled up to VSYS through a 35k $\Omega$ resistor. |
| 10  | PWRHLD  | Power Hold Input. Refer to the <i>Control Sequences</i> section for more information.   |
| 11  | nRSTO   | Active Low Reset Output. See the <i>nRSTO Output</i> section for more information.  |
| 12  | nIRQ    | Open-Drain Interrupt Output. nIRQ is asserted any time an unmasked fault condition exists or a charger interrupt occurs. See the <i>nIRQ Output</i> section for more information.   |
| 13  | nPBSTAT | Active-Low Open-Drain Push-Button Status Output. nPBSTAT is asserted low whenever the nPBIN is pushed, and is high-Z otherwise. See the <i>nPBSTAT Output</i> section for more information.   |
| 14  | GP3     | Power Ground for REG3. Connect GA, GP12, and GP3 together at a single point as close to the IC as possible.   |
| 15  | SW3     | Switching Node Output for REG3.   |
| 16  | VP3     | Power Input for REG3. Bypass to GP3 with a high quality ceramic capacitor placed as close to the IC as possible.  |
| 17  | OUT3    | Output Feedback Sense for REG3.   |
| 18  | PWREN   | Power Enable Input. Refer to the <i>Control Sequences</i> section for more information.   |
| 19  | nLBO    | Low Battery Indicator Output. nLBO is asserted low whenever the voltage at LBI is lower than 1.2V, and is high-Z otherwise. See the <i>Precision Voltage Detector</i> section for more information.   |
| 20  | LBI     | Low Battery Input. The input voltage is compared to 1.2V and the output of this comparison drives nLBO. See the <i>Precision Voltage Detector</i> section for more information.   |
| 21  | ACIN    | AC Input Supply Detection. See the <i>Charge Current Programming</i> section for more information.  |
| 22  | CHGLEV  | Charge Current Selection Input. See the <i>Charge Current Programming</i> section for more information.   |

## PIN DESCRIPTIONS CONT'D

| PIN    | NAME  | DESCRIPTION   |
|--------|-------|---|
| 23     | ISET  | Charge Current Set. Program the charge current by connecting a resistor ( $R_{ISET}$ ) between ISET and GA. See the <i>Charge Current Programming</i> section for more information.   |
| 24     | TH    | Temperature Sensing Input. Connect to battery thermistor. TH is pulled up with a 102 $\mu$ A current internally. See the <i>Battery Temperature Monitoring</i> section for more information.  |
| 25     | VSEL  | Step-Down DC/DCs Output Voltage Selection. Drive to logic low to select default output voltage. Drive to logic high to select secondary output voltage. See the <i>Output Voltage Programming</i> section for more information.               |
| 26     | SCL   | Clock Input for I <sup>2</sup> C Serial Interface.  |
| 27     | SDA   | Data Input for I <sup>2</sup> C Serial Interface. Data is read on the rising edge of SCL.   |
| 28     | nSTAT | Active-Low Open-Drain Charger Status Output. nSTAT has a 8mA (typ) current limit, allowing it to directly drive an indicator LED without additional external components. See the <i>Charge Status Indicator</i> section for more information. |
| 29, 30 | BAT   | Battery Charger Output. Connect this pin directly to the battery anode (+ terminal)   |
| 31, 32 | VSYS  | System Output Pin. Bypass to GA with a 10 $\mu$ F or larger ceramic capacitor.  |
| 33     | CHGIN | Power Input for the Battery Charger. Bypass CHGIN to GA with a capacitor placed as close to the IC as possible. The battery charger is automatically enabled when a valid voltage is present on CHGIN .                                       |
| 34     | OUT2  | Output Feedback Sense for REG2.   |
| 35     | VP2   | Power Input for REG2. Bypass to GP12 with a high quality ceramic capacitor placed as close to the IC as possible.   |
| 36     | SW2   | Switching Node Output for REG2.   |
| 37     | GP12  | Power Ground for REG1 and REG2. Connect GA, GP12 and GP3 together at a single point as close to the IC as possible.   |
| 38     | SW1   | Switching Node Output for REG1.   |
| 39     | VP1   | Power Input for REG1. Bypass to GP12 with a high quality ceramic capacitor placed as close to the IC as possible.   |
| 40     | NC    | No Connect. Not internally connected.   |
| EP     | EP    | Exposed Pad. Must be soldered to ground on PCB.   |

## ABSOLUTE MAXIMUM RATINGS<sup>①</sup>

| PARAMETER   | VALUE                       | UNIT |
|---|-----------------------------|------|
| VP1, VP2 to GP12<br>VP3 to GP3  | -0.3 to + 6                 | V    |
| BAT, VSYS, INL to GA  | -0.3 to + 6                 | V    |
| CHGIN to GA   | -0.3 to + 14                | V    |
| SW1, OUT1 to GP12   | -0.3 to ( $V_{VP1} + 0.3$ ) | V    |
| SW2, OUT2 to GP12   | -0.3 to ( $V_{VP2} + 0.3$ ) | V    |
| SW3, OUT3 to GP3  | -0.3 to ( $V_{VP3} + 0.3$ ) | V    |
| nIRQ, nLBO, nPBSTAT, nRSTO, nSTAT to GA   | -0.3 to + 6                 | V    |
| nPBIN, ACIN, CHGLEV, ISET, LBI, PWRHLD, PWREN, REFBP, SCL, SDA, TH,<br>VSEL to GA                 | -0.3 to ( $V_{SYS} + 0.3$ ) | V    |
| OUT4, OUT5, OUT6, OUT7 to GA  | -0.3 to ( $V_{INL} + 0.3$ ) | V    |
| GP12, GP3 to GA   | -0.3 to + 0.3               | V    |
| Operating Ambient Temperature   | -40 to 85                   | °C   |
| Maximum Junction Temperature  | 125                         | °C   |
| Maximum Power Dissipation<br>TQFN55-40 (Thermal Resistance $\theta_{JA} = 30^{\circ}\text{C/W}$ ) | 2.7                         | W    |
| Storage Temperature   | -65 to 150                  | °C   |
| Lead Temperature (Soldering, 10 sec)  | 300                         | °C   |

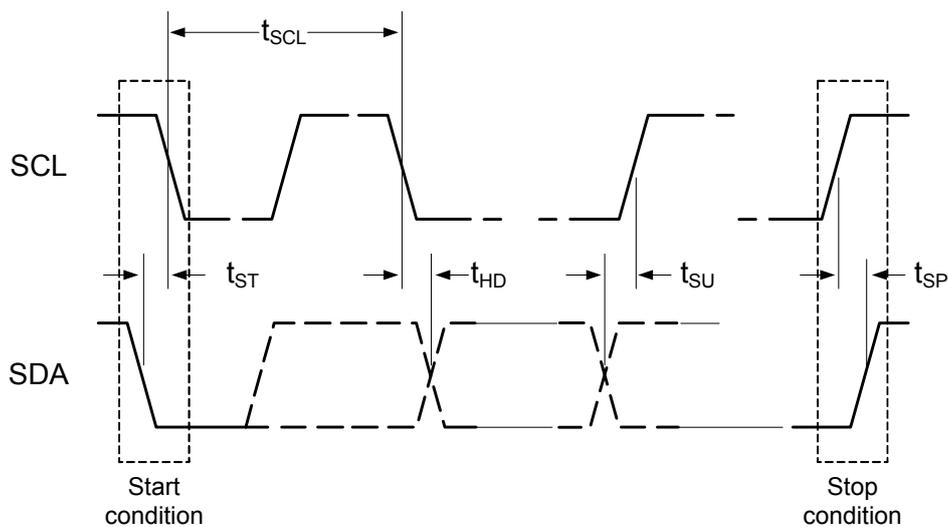
①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

## I<sup>2</sup>C INTERFACE ELECTRICAL CHARACTERISTICS

(V<sub>VSYS</sub> = 3.6V, T<sub>A</sub> = 25°C, unless otherwise specified.)

| PARAMETER                            | TEST CONDITIONS  | MIN  | TYP | MAX  | UNIT |
|--------------------------------------|--|------|-----|------|------|
| SCL, SDA Input Low                   | V <sub>VSYS</sub> = 3.1V to 5.5V, T <sub>A</sub> = -40°C to 85°C |      |     | 0.35 | V    |
| SCL, SDA Input High                  | V <sub>VSYS</sub> = 3.1V to 5.5V, T <sub>A</sub> = -40°C to 85°C | 1.55 |     |      | V    |
| SDA Leakage Current                  |  |      |     | 1    | μA   |
| SCL Leakage Current                  |  |      | 8   | 18   | μA   |
| SDA Output Low                       | I <sub>OL</sub> = 5mA  |      |     | 0.35 | V    |
| SCL Clock Period, t <sub>SCL</sub>   |  | 1.5  |     |      | μs   |
| SDA Data Setup Time, t <sub>SU</sub> |  | 100  |     |      | ns   |
| SDA Data Hold Time, t <sub>HD</sub>  |  | 300  |     |      | ns   |
| Start Setup Time, t <sub>ST</sub>    | For Start Condition  | 100  |     |      | ns   |
| Stop Setup Time, t <sub>SP</sub>     | For Stop Condition   | 100  |     |      | ns   |

**Figure 1:**  
**I<sup>2</sup>C Compatible Serial Bus Timing**



## GLOBAL REGISTER MAP

| OUTPUT | ADDRESS |                      | BITS     |          |            |            |            |            |            |            |
|--------|---------|----------------------|----------|----------|------------|------------|------------|------------|------------|------------|
|        |         |                      | D7       | D6       | D5         | D4         | D3         | D2         | D1         | D0         |
| SYS    | 0x00    | NAME                 | TRST     | nSYSMODE | nSYSLEVMSK | nSYSSTAT   | SYSLEV[3]  | SYSLEV[2]  | SYSLEV[1]  | SYSLEV[0]  |
|        |         | DEFAULT <sup>①</sup> | 0        | 1        | 0          | R          | 0          | 1          | 1          | 1          |
| SYS    | 0x01    | NAME                 | Reserved | Reserved | Reserved   | Reserved   | SCRATCH    | SCRATCH    | SCRATCH    | SCRATCH    |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 0          | 0          | 0          | 0          | 0          | 0          |
| REG1   | 0x20    | NAME                 | Reserved | Reserved | VSET1[5]   | VSET1[4]   | VSET1[3]   | VSET1[2]   | VSET1[1]   | VSET1[0]   |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 1          | 1          | 1          | 0          | 0          | 1          |
| REG1   | 0x21    | NAME                 | Reserved | Reserved | VSET2[5]   | VSET2[4]   | VSET2[3]   | VSET2[2]   | VSET2[1]   | VSET2[0]   |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 1          | 1          | 1          | 0          | 0          | 1          |
| REG1   | 0x22    | NAME                 | ON       | PHASE    | MODE       | DELAY[2]   | DELAY[1]   | DELAY[0]   | nFLTMSK    | OK         |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 0          | 0          | 1          | 1          | 0          | R          |
| REG2   | 0x30    | NAME                 | Reserved | Reserved | VSET1[5]   | VSET1[4]   | VSET1[3]   | VSET1[2]   | VSET1[1]   | VSET1[0]   |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 0          | 1          | 0          | 1          | 0          | 0          |
| REG2   | 0x31    | NAME                 | Reserved | Reserved | VSET2[5]   | VSET2[4]   | VSET2[3]   | VSET2[2]   | VSET2[1]   | VSET2[0]   |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 0          | 1          | 0          | 1          | 0          | 0          |
| REG2   | 0x32    | NAME                 | ON       | PHASE    | MODE       | DELAY[2]   | DELAY[1]   | DELAY[0]   | nFLTMSK    | OK         |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 0          | 0          | 1          | 1          | 0          | R          |
| REG3   | 0x40    | NAME                 | Reserved | Reserved | VSET1[5]   | VSET1[4]   | VSET1[3]   | VSET1[2]   | VSET1[1]   | VSET1[0]   |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 0          | 1          | 1          | 0          | 0          | 1          |
| REG3   | 0x41    | NAME                 | Reserved | Reserved | VSET2[5]   | VSET2[4]   | VSET2[3]   | VSET2[2]   | VSET2[1]   | VSET2[0]   |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 0          | 1          | 1          | 0          | 0          | 1          |
| REG3   | 0x42    | NAME                 | ON       | Reserved | MODE       | DELAY[2]   | DELAY[1]   | DELAY[0]   | nFLTMSK    | OK         |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 0          | 0          | 1          | 1          | 0          | R          |
| REG4   | 0x50    | NAME                 | Reserved | Reserved | VSET[5]    | VSET[4]    | VSET[3]    | VSET[2]    | VSET[1]    | VSET[0]    |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 0          | 1          | 0          | 1          | 0          | 0          |
| REG4   | 0x51    | NAME                 | ON       | DIS      | LOWIQ      | DELAY[2]   | DELAY[1]   | DELAY[0]   | nFLTMSK    | OK         |
|        |         | DEFAULT <sup>①</sup> | 0        | 1        | 0          | 0          | 1          | 1          | 0          | R          |
| REG5   | 0x54    | NAME                 | Reserved | Reserved | VSET[5]    | VSET[4]    | VSET[3]    | VSET[2]    | VSET[1]    | VSET[0]    |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 0          | 1          | 0          | 1          | 0          | 0          |
| REG5   | 0x55    | NAME                 | ON       | DIS      | LOWIQ      | DELAY[2]   | DELAY[1]   | DELAY[0]   | nFLTMSK    | OK         |
|        |         | DEFAULT <sup>①</sup> | 0        | 1        | 0          | 0          | 0          | 0          | 0          | R          |
| REG6   | 0x60    | NAME                 | Reserved | Reserved | VSET[5]    | VSET[4]    | VSET[3]    | VSET[2]    | VSET[1]    | VSET[0]    |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 0          | 1          | 0          | 1          | 0          | 0          |
| REG6   | 0x61    | NAME                 | ON       | DIS      | LOWIQ      | DELAY[2]   | DELAY[1]   | DELAY[0]   | nFLTMSK    | OK         |
|        |         | DEFAULT <sup>①</sup> | 0        | 1        | 0          | 0          | 1          | 1          | 0          | R          |
| REG7   | 0x64    | NAME                 | Reserved | Reserved | VSET[5]    | VSET[4]    | VSET[3]    | VSET[2]    | VSET[1]    | VSET[0]    |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 1          | 1          | 1          | 0          | 0          | 1          |
| REG7   | 0x65    | NAME                 | ON       | DIS      | LOWIQ      | DELAY[2]   | DELAY[1]   | DELAY[0]   | nFLTMSK    | OK         |
|        |         | DEFAULT <sup>①</sup> | 0        | 1        | 0          | 1          | 0          | 0          | 0          | R          |
| APCH   | 0x70    | NAME                 | Reserved | Reserved | Reserved   | Reserved   | Reserved   | Reserved   | Reserved   | Reserved   |
|        |         | DEFAULT <sup>①</sup> | 0        | 1        | 0          | 1          | 0          | 0          | 0          | 0          |
| APCH   | 0x71    | NAME                 | SUSCHG   | Reserved | TOTTIMO[1] | TOTTIMO[0] | PRETIMO[1] | PRETIMO[0] | OVPSSET[1] | OVPSSET[0] |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 1          | 0          | 1          | 0          | 0          | 0          |
| APCH   | 0x78    | NAME                 | TIMRSTAT | TEMPSTAT | INSTAT     | CHGSTAT    | TIMRDAT    | TEMPDAT    | INDAT      | CHGDAT     |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 0          | 0          | R          | R          | R          | R          |
| APCH   | 0x79    | NAME                 | TIMRTOT  | TEMPIN   | INCON      | CHGEOCIN   | TIMRPRE    | TEMPOUT    | INDIS      | CHGEOCOUT  |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | 0          | 0          | 0          | 0          | 0          | 0          |
| APCH   | 0x7A    | NAME                 | Reserved | Reserved | CSTATE[0]  | CSTATE[1]  | Reserved   | Reserved   | ACINSTAT   | Reserved   |
|        |         | DEFAULT <sup>①</sup> | 0        | 0        | R          | R          | R          | R          | R          | R          |

①: Default values of ACT8937QJ21C-T.

②: All bits are automatically cleared to default values when the input power is removed or falls below the system UVLO.

## REGISTER AND BIT DESCRIPTIONS

**Table 1:**  
**Global Register Map**

| OUTPUT | ADDRESS | BIT   | NAME       | ACCESS | DESCRIPTION   |
|--------|---------|-------|------------|--------|---|
| SYS    | 0x00    | [7]   | TRST       | R/W    | Reset Timer Setting. Defines the reset time-out threshold. Reset time-out is 65ms when value is 1, reset time-out is 260ms when value is 0. See <i>nRSTO Output</i> section for more information.   |
| SYS    | 0x00    | [6]   | nSYSMODE   | R/W    | SYSLEV Mode Select. Defines the response to the SYSLEV voltage detector, 1: Generate an interrupt when $V_{V_{SYS}}$ falls below the programmed SYSLEV threshold, 0: automatic shutdown when $V_{V_{SYS}}$ falls below the programmed SYSLEV threshold. |
| SYS    | 0x00    | [5]   | nSYSLEVMSK | R/W    | System Voltage Level Interrupt Mask. SYSLEV interrupt is masked by default, set to 1 to unmask this interrupt. See the <i>Programmable System Voltage Monitor</i> section for more information  |
| SYS    | 0x00    | [4]   | nSYSSTAT   | R      | System Voltage Status. Value is 1 when $V_{V_{SYS}}$ is lower than the SYSLEV voltage threshold, value is 0 when $V_{V_{SYS}}$ is higher than the system voltage detection threshold.   |
| SYS    | 0x00    | [3:0] | SYSLEV     | R/W    | System Voltage Detect Threshold. Defines the SYSLEV voltage threshold. See the <i>Programmable System Voltage Monitor</i> section for more information.   |
| SYS    | 0x01    | [7:4] | -          | R/W    | Reserved.   |
| SYS    | 0x01    | [3:0] | SCRATCH    | R/W    | Scratchpad Bits. Non-functional bits, maybe be used by user to store system status information. Volatile bits, which are cleared when system voltage falls below UVLO threshold.  |
| REG1   | 0x20    | [7:6] | -          | R      | Reserved.   |
| REG1   | 0x20    | [5:0] | VSET1      | R/W    | Primary Output Voltage Selection. Valid when VSEL is driven low. See the <i>Output Voltage Programming</i> section for more information.  |
| REG1   | 0x21    | [7:6] | -          | R      | Reserved.   |
| REG1   | 0x21    | [5:0] | VSET2      | R/W    | Secondary Output Voltage Selection. Valid when VSEL is driven high. See the <i>Output Voltage Programming</i> section for more information.   |
| REG1   | 0x22    | [7]   | ON         | R/W    | Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.  |
| REG1   | 0x22    | [6]   | PHASE      | R/W    | Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.   |
| REG1   | 0x22    | [5]   | MODE       | R/W    | Regulator Mode Select. Set bit to 1 for fixed-frequency PWM under all load conditions, clear bit to 0 to transit to power-savings mode under light-load conditions.   |
| REG1   | 0x22    | [4:2] | DELAY      | R/W    | Regulator Turn-On Delay Control. See the <i>REG1, REG2, REG3 Turn-on Delay</i> section for more information.  |
| REG1   | 0x22    | [1]   | nFLTMSK    | R/W    | Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.   |
| REG1   | 0x22    | [0]   | OK         | R      | Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.   |
| REG2   | 0x30    | [7:6] | -          | R      | Reserved.   |
| REG2   | 0x30    | [5:0] | VSET1      | R/W    | Primary Output Voltage Selection. Valid when VSEL is driven low. See the <i>Output Voltage Programming</i> section for more information.  |
| REG2   | 0x31    | [7:6] | -          | R      | Reserved.   |

**REGISTER AND BIT DESCRIPTIONS CONT'D**

| OUTPUT | ADDRESS | BIT   | NAME    | ACCESS | DESCRIPTION   |
|--------|---------|-------|---------|--------|---|
| REG2   | 0x31    | [5:0] | VSET2   | R/W    | Secondary Output Voltage Selection. Valid when VSEL is driven high. See the <i>Output Voltage Programming</i> section for more information.   |
| REG2   | 0x32    | [7]   | ON      | R/W    | Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.  |
| REG2   | 0x32    | [6]   | PHASE   | R/W    | Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.                                     |
| REG2   | 0x32    | [5]   | MODE    | R/W    | Regulator Mode Select. Set bit to 1 for fixed-frequency PWM under all load conditions, clear bit to 0 to transit to power-savings mode under light-load conditions.   |
| REG2   | 0x32    | [4:2] | DELAY   | R/W    | Regulator Turn-On Delay Control. See the <i>REG1, REG2, REG3 Turn-on Delay</i> section for more information.  |
| REG2   | 0x32    | [1]   | nFLTMSK | R/W    | Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.   |
| REG2   | 0x32    | [0]   | OK      | R      | Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.   |
| REG3   | 0x40    | [7:6] | -       | R      | Reserved.   |
| REG3   | 0x40    | [5:0] | VSET1   | R/W    | Primary Output Voltage Selection. Valid when VSEL is driven low. See the <i>Output Voltage Programming</i> section for more information.  |
| REG3   | 0x41    | [7:6] | -       | R      | Reserved.   |
| REG3   | 0x41    | [5:0] | VSET2   | R/W    | Secondary Output Voltage Selection. Valid when VSEL is driven high. See the <i>Output Voltage Programming</i> section for more information.   |
| REG3   | 0x42    | [7]   | ON      | R/W    | Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.  |
| REG3   | 0x42    | [6]   | -       | R/W    | Reserved.   |
| REG3   | 0x42    | [5]   | MODE    | R/W    | Regulator Mode Select. Set bit to 1 for fixed-frequency PWM under all load conditions, clear bit to 0 to transit to power-savings mode under light-load conditions.   |
| REG3   | 0x42    | [4:2] | DELAY   | R/W    | Regulator Turn-On Delay Control. See the <i>REG1, REG2, REG3 Turn-on Delay</i> section for more information.  |
| REG3   | 0x42    | [1]   | nFLTMSK | R/W    | Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.   |
| REG3   | 0x42    | [0]   | OK      | R      | Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.   |
| REG4   | 0x50    | [7:6] | -       | R      | Reserved.   |
| REG4   | 0x50    | [5:0] | VSET    | R/W    | Output Voltage Selection. See the <i>Output Voltage Programming</i> section for more information.   |
| REG4   | 0x51    | [7]   | ON      | R/W    | Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.  |
| REG4   | 0x51    | [6]   | DIS     | R/W    | Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function. |
| REG4   | 0x51    | [5]   | LOWIQ   | R/W    | LDO Low-IQ Mode Control. Set bit to 1 for low-power operating mode, clear bit to 0 for normal mode.   |
| REG4   | 0x51    | [4:2] | DELAY   | R/W    | Regulator Turn-On Delay Control. See the <i>REG4, REG5, REG6, REG7 Turn-on Delay</i> section for more information.  |
| REG4   | 0x51    | [1]   | nFLTMSK | R/W    | Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.   |

## REGISTER AND BIT DESCRIPTIONS CONT'D

| OUTPUT | ADDRESS | BIT   | NAME    | ACCESS | DESCRIPTION   |
|--------|---------|-------|---------|--------|---|
| REG4   | 0x51    | [0]   | OK      | R      | Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.   |
| REG5   | 0x54    | [7:6] | -       | R      | Reserved.   |
| REG5   | 0x54    | [5:0] | VSET    | R/W    | Output Voltage Selection. See the <i>Output Voltage Programming</i> section for more information.   |
| REG5   | 0x55    | [7]   | ON      | R/W    | Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.  |
| REG5   | 0x55    | [6]   | DIS     | R/W    | Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function. |
| REG5   | 0x55    | [5]   | LOWIQ   | R/W    | LDO Low-IQ Mode Control. Set bit to 1 for low-power operating mode, clear bit to 0 for normal mode.   |
| REG5   | 0x55    | [4:2] | DELAY   | R/W    | Regulator Turn-On Delay Control. See the <i>REG4, REG5, REG6, REG7 Turn-on Delay</i> section for more information.  |
| REG5   | 0x55    | [1]   | nFLTMSK | R/W    | Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.   |
| REG5   | 0x55    | [0]   | OK      | R      | Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.   |
| REG6   | 0x60    | [7:6] | -       | R      | Reserved.   |
| REG6   | 0x60    | [5:0] | VSET    | R/W    | Output Voltage Selection. See the <i>Output Voltage Programming</i> section for more information.   |
| REG6   | 0x61    | [7]   | ON      | R/W    | Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.  |
| REG6   | 0x61    | [6]   | DIS     | R/W    | Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function. |
| REG6   | 0x61    | [5]   | LOWIQ   | R/W    | LDO Low-IQ Mode Control. Set bit to 1 for low-power operating mode, clear bit to 0 for normal mode.   |
| REG6   | 0x61    | [4:2] | DELAY   | R/W    | Regulator Turn-On Delay Control. See the <i>REG4, REG5, REG6, REG7 Turn-on Delay</i> section for more information.  |
| REG6   | 0x61    | [1]   | nFLTMSK | R/W    | Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.   |
| REG6   | 0x61    | [0]   | OK      | R      | Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.   |
| REG7   | 0x64    | [7:6] | -       | R      | Reserved.   |
| REG7   | 0x64    | [5:0] | VSET    | R/W    | Output Voltage Selection. See the <i>Output Voltage Programming</i> section for more information.   |
| REG7   | 0x65    | [7]   | ON      | R/W    | Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.  |
| REG7   | 0x65    | [6]   | DIS     | R/W    | Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function. |
| REG7   | 0x65    | [5]   | LOWIQ   | R/W    | LDO Low-IQ Mode Control. Set bit to 1 for low-power operating mode, clear bit to 0 for normal mode.   |
| REG7   | 0x65    | [4:2] | DELAY   | R/W    | Regulator Turn-On Delay Control. See the <i>REG4, REG5, REG6, REG7 Turn-on Delay</i> section for more information.  |
| REG7   | 0x65    | [1]   | nFLTMSK | R/W    | Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.   |

## REGISTER AND BIT DESCRIPTIONS CONT'D

| OUTPUT | ADDRESS | BIT   | NAME                  | ACCESS | DESCRIPTION   |
|--------|---------|-------|-----------------------|--------|---|
| REG7   | 0x65    | [0]   | OK                    | R      | Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.   |
| APCH   | 0x70    | [7:0] | -                     | R/W    | Reserved.   |
| APCH   | 0x71    | [7]   | SUSCHG                | R/W    | Charge Suspend Control Input. Set bit to 1 to suspend charging, clear bit to 0 to allow charging to resume.   |
| APCH   | 0x71    | [6]   | -                     | R/W    | Reserved.   |
| APCH   | 0x71    | [5:4] | TOTTIMO               | R/W    | Total Charge Time-out Selection. See the <i>Charge Safety Timers</i> section for more information.  |
| APCH   | 0x71    | [3:2] | PRETIMO               | R/W    | Precondition Charge Time-out Selection. See the <i>Charge Safety Timers</i> section for more information.   |
| APCH   | 0x71    | [1:0] | OVPSET                | R/W    | Input Over-Voltage Protection Threshold Selection. See the <i>Input Over-Voltage Protection</i> section for more information.   |
| APCH   | 0x78    | [7]   | TIMRSTAT <sup>Ⓣ</sup> | R/W    | Charge Time-out Interrupt Status. Set this bit with TIMRPRE[ ] and/or TIMRTOT[ ] to 1 to generate an interrupt when charge safety timers expire, read this bit to get charge time-out interrupt status. See the <i>Charge Safety Timers</i> section for more information.                             |
| APCH   | 0x78    | [6]   | TEMPSTAT <sup>Ⓣ</sup> | R/W    | Battery Temperature Interrupt Status. Set this bit with TEMPIN[ ] and/or TEMPOUT[ ] to 1 to generate an interrupt when a battery temperature event occurs, read this bit to get the battery temperature interrupt status. See the <i>Battery Temperature Monitoring</i> section for more information. |
| APCH   | 0x78    | [5]   | INSTAT                | R/W    | Input Voltage Interrupt Status. Set this bit with INCON[ ] and/or INDIS[ ] to generate an interrupt when UVLO or OVP condition occurs, read this bit to get the input voltage interrupt status. See the <i>Charge Current Programming</i> section for more information.                               |
| APCH   | 0x78    | [4]   | CHGSTAT <sup>Ⓣ</sup>  | R/W    | Charge State Interrupt Status. Set this bit with CHGEOCIN[ ] and/or CHGEOCOUT[ ] to 1 to generate an interrupt when the state machine gets in or out of EOC state, read this bit to get the charger state interrupt status. See the <i>State Machine Interrupts</i> section for more information.     |
| APCH   | 0x78    | [3]   | TIMRDAT <sup>Ⓣ</sup>  | R      | Charge Timer Status. Value is 1 when precondition time-out or total charge time-out occurs. Value is 0 in other case.   |
| APCH   | 0x78    | [2]   | TEMPDAT <sup>Ⓣ</sup>  | R      | Temperature Status. Value is 0 when battery temperature is outside of valid range. Value is 1 when battery temperature is inside of valid range.  |
| APCH   | 0x78    | [1]   | INDAT                 | R      | Input Voltage Status. Value is 1 when a valid input at CHGIN is present. Value is 0 when a valid input at CHGIN is not present.   |
| APCH   | 0x78    | [0]   | CHGDAT <sup>Ⓣ</sup>   | R      | Charge State Machine Status. Value is 1 indicates the charger state machine is in EOC state, value is 0 indicates the charger state machine is in other states.   |
| APCH   | 0x79    | [7]   | TIMRTOT               | R/W    | Total Charge Time-out Interrupt control. Set both this bit and TIMRSTAT[ ] to 1 to generate an interrupt when a total charge time-out occurs. See the <i>Charge Safety Timers</i> section for more information.   |
| APCH   | 0x79    | [6]   | TEMPIN                | R/W    | Battery Temperature Interrupt Control. Set both this bit and TEMPSTAT[ ] to 1 to generate an interrupt when the battery temperature goes into the valid range. See the <i>Battery Temperature Monitoring</i> section for more information.  |

Ⓣ: Valid only when CHGIN UVLO Threshold < V<sub>CHGIN</sub> < CHGIN OVP Threshold.

## REGISTER AND BIT DESCRIPTIONS CONT'D

| OUTPUT | ADDRESS | BIT   | NAME      | ACCESS | DESCRIPTION  |
|--------|---------|-------|-----------|--------|--|
| APCH   | 0x79    | [5]   | INCON     | R/W    | Input Voltage Interrupt Control. Set both this bit and INSTAT[ ] to 1 to generate an interrupt when CHGIN input voltage goes into the valid range. See the <i>Charge Current Programming</i> section for more information.                   |
| APCH   | 0x79    | [4]   | CHGEOCIN  | R/W    | Charge State Interrupt Control. Set both this bit and CHGSTAT[ ] to 1 to generate an interrupt when the state machine goes into the EOC state. See the <i>State Machine Interrupts</i> section for more information.                         |
| APCH   | 0x79    | [3]   | TIMRPRE   | R/W    | PRECHARGE Time-out Interrupt control. Set both this bit and TIMRSTAT[ ] to 1 to generate an interrupt when a PRECHARGE time-out occurs. See the <i>Charge Safety Timers</i> section for more information.                                    |
| APCH   | 0x79    | [2]   | TEMPOUT   | R/W    | Battery Temperature Interrupt Control. Set both this bit and TEMPSTAT[ ] to 1 to generate an interrupt when the battery temperature goes out of the valid range. See the <i>Battery Temperature Monitoring</i> section for more information. |
| APCH   | 0x79    | [1]   | INDIS     | R/W    | Input Voltage Interrupt Control. Set both this bit and INSTAT[ ] to 1 to generate an interrupt when CHGIN input voltage goes out of the valid range. See the <i>Charge Current Programming</i> section for more information.                 |
| APCH   | 0x79    | [0]   | CHGEOCOUT | R/W    | Charge State Interrupt Control. Set both this bit and CHGSTAT[ ] to 1 to generate an interrupt when the state machines jumps out of the EOC state. See the <i>State Machine Interrupts</i> section for more information.                     |
| APCH   | 0x7A    | [7:6] | -         | R      | Reserved.  |
| APCH   | 0x7A    | [5:4] | CSTATE    | R      | Charge State. Values indicate the current charging state. See the <i>State Machine Interrupts</i> section for more information.  |
| APCH   | 0x7A    | [3:2] | -         | R      | Reserved.  |
| APCH   | 0x7A    | [1]   | ACINSTAT  | R      | ACIN Status. Indicates the state of the ACIN input, typically in order to identify the type of input supply connected. Value is 1 when ACIN is above the 1.2V precision threshold, value is 0 when ACIN is below this threshold.             |
| APCH   | 0x7A    | [0]   | -         | R      | Reserved.  |

## SYSTEM CONTROL ELECTRICAL CHARACTERISTICS

( $V_{SYS} = 3.6V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.)

| PARAMETER                             | TEST CONDITIONS   | MIN  | TYP              | MAX  | UNIT       |
|---------------------------------------|---|------|------------------|------|------------|
| Input Voltage Range                   |   | 2.7  |                  | 5.5  | V          |
| UVLO Threshold Voltage                | $V_{SYS}$ Rising  | 2.2  | 2.45             | 2.65 | V          |
| UVLO Hysteresis                       | $V_{SYS}$ Falling   |      | 200              |      | mV         |
| Supply Current                        | REG1 and REG5 Enabled. REG2, REG3, REG4, REG6 and REG7 Disabled |      | 190              |      | $\mu A$    |
|                                       | REG1, REG2, REG3, REG4 and REG5 Enabled. REG6 and REG7 Disabled |      | 340              |      |            |
|                                       | REG1, REG2, REG3, REG4, REG5, REG6 and REG7 Enabled             |      | 420              |      |            |
| Shutdown Supply Current               | All Regulators Disabled   |      | 8                | 18   | $\mu A$    |
| Oscillator Frequency                  |   | 1.8  | 2                | 2.2  | MHz        |
| Logic High Input Voltage <sup>①</sup> |   | 1.4  |                  |      | V          |
| Logic Low Input Voltage               |   |      |                  | 0.4  | V          |
| Leakage Current                       | $V_{nIRQ} = V_{nRSTO} = 4.2V$                                   |      |                  | 1    | $\mu A$    |
| LBI Threshold Voltage                 | $V_{BAT}$ Falling   | 1.03 | 1.2              | 1.31 | V          |
| LBI Hysteresis Threshold              | $V_{BAT}$ Rising  |      | 200              |      | mV         |
| Low Level Output Voltage <sup>②</sup> | $I_{SINK} = 5mA$  |      |                  | 0.35 | V          |
| nRSTO Delay                           |   |      | 260 <sup>③</sup> |      | ms         |
| Thermal Shutdown Temperature          | Temperature rising  |      | 160              |      | $^\circ C$ |
| Thermal Shutdown Hysteresis           |   |      | 20               |      | $^\circ C$ |

①: PWRHLD, PWREN, VSEL are logic inputs.

②: nLBO, nPBSTAT, nIRQ, nRSTO are open drain outputs.

③: Typical value shown. Actual value may vary from 227.9ms to 291.2ms.

## STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS

( $V_{VP1} = V_{VP2} = V_{VP3} = 3.6V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.)

| PARAMETER                | CONDITIONS   | MIN | TYP                         | MAX | UNIT        |
|--------------------------|--|-----|-----------------------------|-----|-------------|
| Operating Voltage Range  |  | 2.7 |                             | 5.5 | V           |
| UVLO Threshold           | Input Voltage Rising   | 2.5 | 2.6                         | 2.7 | V           |
| UVLO Hysteresis          | Input Voltage Falling  |     | 100                         |     | mV          |
| Quiescent Supply Current | Regulator Enabled  |     | 65                          | 90  | $\mu A$     |
| Shutdown Current         | $V_{VP} = 5.5V$ , Regulator Disabled                               |     | 0                           | 1   | $\mu A$     |
| Output Voltage Accuracy  | $V_{OUT} \geq 1.2V$ , $I_{OUT} = 10mA$                             | -1% | $V_{NOM}^{\textcircled{1}}$ | 1%  | V           |
|                          | $V_{OUT} < 1.2V$ , $I_{OUT} = 10mA$                                | -2% | $V_{NOM}^{\textcircled{1}}$ | 2%  |             |
| Line Regulation          | $V_{VP} = \text{Max}(V_{NOM}^{\textcircled{1}} + 1, 3.2V)$ to 5.5V |     | 0.15                        |     | %/V         |
| Load Regulation          | $I_{OUT} = 10mA$ to $I_{MAX}^{\textcircled{2}}$                    |     | 0.0017                      |     | %/mA        |
| Power Good Threshold     | $V_{OUT}$ Rising   |     | 93                          |     | % $V_{NOM}$ |
| Power Good Hysteresis    | $V_{OUT}$ Falling  |     | 2                           |     | % $V_{NOM}$ |
| Oscillator Frequency     | $V_{OUT} \geq 20\%$ of $V_{NOM}$                                   | 1.8 | 2                           | 2.2 | MHz         |
|                          | $V_{OUT} = 0V$   |     | 500                         |     | kHz         |
| Soft-Start Period        |  |     | 400                         |     | $\mu s$     |
| Minimum On-Time          |  |     | 75                          |     | ns          |
| <b>REG1</b>              |  |     |                             |     |             |
| Maximum Output Current   |  | 1.1 |                             |     | A           |
| Current Limit            |  | 1.5 | 1.8                         | 2.1 | A           |
| PMOS On-Resistance       | $I_{SW1} = -100mA$   |     | 0.16                        |     | $\Omega$    |
| NMOS On-Resistance       | $I_{SW1} = 100mA$  |     | 0.16                        |     | $\Omega$    |
| SW1 Leakage Current      | $V_{VP1} = 5.5V$ , $V_{SW1} = 0$ or 5.5V                           |     | 0                           | 1   | $\mu A$     |
| <b>REG2</b>              |  |     |                             |     |             |
| Maximum Output Current   |  | 1.1 |                             |     | A           |
| Current Limit            |  | 1.5 | 1.8                         | 2.1 | A           |
| PMOS On-Resistance       | $I_{SW2} = -100mA$   |     | 0.16                        |     | $\Omega$    |
| NMOS On-Resistance       | $I_{SW2} = 100mA$  |     | 0.16                        |     | $\Omega$    |
| SW2 Leakage Current      | $V_{VP2} = 5.5V$ , $V_{SW2} = 0$ or 5.5V                           |     | 0                           | 1   | $\mu A$     |
| <b>REG3</b>              |  |     |                             |     |             |
| Maximum Output Current   |  | 1.2 |                             |     | A           |
| Current Limit            |  | 1.5 | 1.8                         | 2.1 | A           |
| PMOS On-Resistance       | $I_{SW3} = -100mA$   |     | 0.16                        |     | $\Omega$    |
| NMOS On-Resistance       | $I_{SW3} = 100mA$  |     | 0.16                        |     | $\Omega$    |
| SW3 Leakage Current      | $V_{VP3} = 5.5V$ , $V_{SW3} = 0$ or 5.5V                           |     | 0                           | 1   | $\mu A$     |

$\textcircled{1}$ :  $V_{NOM}$  refers to the nominal output voltage level for  $V_{OUT}$  as defined by the *Ordering Information* section.

$\textcircled{2}$ :  $I_{MAX}$  Maximum Output Current.

## LOW-NOISE LDO ELECTRICAL CHARACTERISTICS

( $V_{INL} = 3.6V$ ,  $C_{OUT4} = C_{OUT5} = 1.5\mu F$ ,  $C_{OUT6} = C_{OUT7} = 2.2\mu F$ ,  $LOWIQ[ ] = [0]$ ,  $T_A = 25^\circ C$ , unless otherwise specified.)

| PARAMETER                    | TEST CONDITIONS  | MIN | TYP                         | MAX | UNIT          |
|------------------------------|--|-----|-----------------------------|-----|---------------|
| Operating Voltage Range      |  | 2.5 |                             | 5.5 | V             |
| Output Voltage Accuracy      | $V_{OUT} \geq 1.2V$ , $T_A = 25^\circ C$ , $I_{OUT} = 10mA$              | -1% | $V_{NOM}^{\textcircled{1}}$ | 2%  | V             |
|                              | $V_{OUT} < 1.2V$ , $T_A = 25^\circ C$ , $I_{OUT} = 10mA$                 | -2% | $V_{NOM}^{\textcircled{1}}$ | 4%  |               |
| Line Regulation              | $V_{INL} = \text{Max}(V_{OUT} + 0.5V, 3.6V)$ to 5.5V<br>$LOWIQ[ ] = [0]$ |     | 0.05                        |     | mV/V          |
|                              | $V_{INL} = \text{Max}(V_{OUT} + 0.5V, 3.6V)$ to 5.5V<br>$LOWIQ[ ] = [1]$ |     | 0.5                         |     |               |
| Load Regulation              | $I_{OUT} = 1mA$ to $IMAX^{\textcircled{2}}$                              |     | 0.08                        |     | V/A           |
| Power Supply Rejection Ratio | $f = 1kHz$ , $I_{OUT} = 20mA$ , $V_{OUT} = 1.2V$                         |     | 75                          |     | dB            |
|                              | $f = 10kHz$ , $I_{OUT} = 20mA$ , $V_{OUT} = 1.2V$                        |     | 65                          |     |               |
| Supply Current per Output    | Regulator Enabled, $LOWIQ[ ] = [0]$                                      |     | 37                          | 60  | $\mu A$       |
|                              | Regulator Enabled, $LOWIQ[ ] = [1]$                                      |     | 31                          | 52  |               |
|                              | Regulator Disabled   |     | 0                           | 1   |               |
| Soft-Start Period            | $V_{OUT} = 2.9V$   |     | 140                         |     | $\mu s$       |
| Power Good Threshold         | $V_{OUT}$ Rising   |     | 89                          |     | %             |
| Power Good Hysteresis        | $V_{OUT}$ Falling  |     | 3                           |     | %             |
| Output Noise                 | $I_{OUT} = 20mA$ , $f = 10Hz$ to $100kHz$ , $V_{OUT} = 1.2V$             |     | 50                          |     | $\mu V_{RMS}$ |
| Discharge Resistance         | LDO Disabled, $DIS[ ] = 1$   |     | 1.5                         |     | $k\Omega$     |
| <b>REG4</b>                  |  |     |                             |     |               |
| Dropout Voltage <sup>③</sup> | $I_{OUT} = 80mA$ , $V_{OUT} > 3.1V$                                      |     | 90                          | 180 | mV            |
| Maximum Output Current       |  | 150 |                             |     | mA            |
| Current Limit <sup>④</sup>   | $V_{OUT} = 95\%$ of regulation voltage                                   | 200 |                             |     | mA            |
| Stable $C_{OUT4}$ Range      |  | 1.5 |                             | 20  | $\mu F$       |
| <b>REG5</b>                  |  |     |                             |     |               |
| Dropout Voltage              | $I_{OUT} = 80mA$ , $V_{OUT} > 3.1V$                                      |     | 140                         | 280 | mV            |
| Maximum Output Current       |  | 150 |                             |     | mA            |
| Current Limit                | $V_{OUT} = 95\%$ of regulation voltage                                   | 200 |                             |     | mA            |
| Stable $C_{OUT5}$ Range      |  | 1.5 |                             | 20  | $\mu F$       |
| <b>REG6</b>                  |  |     |                             |     |               |
| Dropout Voltage              | $I_{OUT} = 120mA$ , $V_{OUT} > 3.1V$                                     |     | 90                          | 180 | mV            |
| Maximum Output Current       |  | 250 |                             |     | mA            |
| Current Limit                | $V_{OUT} = 95\%$ of regulation voltage                                   | 300 |                             |     | mA            |
| Stable $C_{OUT6}$ Range      |  | 2.2 |                             | 20  | $\mu F$       |
| <b>REG7</b>                  |  |     |                             |     |               |
| Dropout Voltage              | $I_{OUT} = 120mA$ , $V_{OUT} > 3.1V$                                     |     | 140                         | 280 | mV            |
| Maximum Output Current       |  | 250 |                             |     | mA            |
| Current Limit                | $V_{OUT} = 95\%$ of regulation voltage                                   | 300 |                             |     | mA            |
| Stable $C_{OUT7}$ Range      |  | 2.2 |                             | 20  | $\mu F$       |

①:  $V_{NOM}$  refers to the nominal output voltage level for  $V_{OUT}$  as defined by the *Ordering Information* section.

②:  $IMAX$  Maximum Output Current.

③: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage (for 3.1V output voltage or higher).

④: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 30% (typ)

## ActivePath™ CHARGER ELECTRICAL CHARACTERISTICS

(V<sub>CHGIN</sub> = 5.0V, T<sub>A</sub> = 25°C, unless otherwise specified.)

| PARAMETER   | TEST CONDITIONS  | MIN  | TYP  | MAX  | UNIT |
|---|--|------|------|------|------|
| <b>ActivePath</b>   |  |      |      |      |      |
| CHGIN Operating Voltage Range   |  | 4.35 |      | 6.0  | V    |
| CHGIN UVLO Threshold  | CHGIN Voltage Rising   | 3.1  | 3.5  | 3.9  | V    |
| CHGIN UVLO Hysteresis   | CHGIN Voltage Falling  |      | 0.5  |      | V    |
| CHGIN OVP Threshold   | CHGIN Voltage Rising   | 6.0  | 6.6  | 7.2  | V    |
| CHGIN OVP Hysteresis  | CHGIN Voltage Falling  |      | 0.4  |      | V    |
| CHGIN Supply Current  | V <sub>CHGIN</sub> < V <sub>UVLO</sub>   |      | 35   | 70   | μA   |
|   | V <sub>CHGIN</sub> < V <sub>BAT</sub> + 50mV, V <sub>CHGIN</sub> > V <sub>UVLO</sub>   |      | 100  | 200  | μA   |
|   | V <sub>CHGIN</sub> > V <sub>BAT</sub> + 150mV, V <sub>CHGIN</sub> > V <sub>UVLO</sub><br>Charger disabled, I <sub>VSYS</sub> = 0mA |      | 1.3  | 2.0  | mA   |
| CHGIN to VSYS On-Resistance   | I <sub>VSYS</sub> = 100mA  |      | 0.3  |      | Ω    |
| CHGIN to VSYS Current Limit   | ACIN = VSYS  | 1.5  | 2    |      | A    |
|   | ACIN = GA, CHGLEV = GA   | 80   | 90   | 100  | mA   |
|   | ACIN = GA, CHGLEV = VSYS   | 400  | 450  | 500  |      |
| <b>VSYS REGULATION</b>  |  |      |      |      |      |
| VSYS Regulated Voltage  | I <sub>VSYS</sub> = 10mA   | 4.45 | 4.6  | 4.8  | V    |
| <b>nSTAT OUTPUT</b>   |  |      |      |      |      |
| nSTAT Sink current  | V <sub>nSTAT</sub> = 2V  | 4    | 8    | 12   | mA   |
| nSTAT Leakage Current   | V <sub>nSTAT</sub> = 4.2V  |      |      | 1    | μA   |
| <b>ACIN AND CHGLEV INPUTS</b>   |  |      |      |      |      |
| CHGLEV Logic High Input Voltage   |  | 1.4  |      |      | V    |
| CHGLEV Logic Low Input Voltage  |  |      |      | 0.4  | V    |
| CHGLEV Leakage Current  | V <sub>CHGLEV</sub> = 4.2V   |      |      | 1    | μA   |
| ACIN Voltage Thresholds   | ACIN voltage rising  | 1.03 | 1.2  | 1.31 | V    |
| ACIN Hysteresis voltage threshold                                       | ACIN voltage falling   |      | 200  |      | mV   |
| ACIN Leakage Current  | V <sub>ACIN</sub> = 4.2V   |      |      | 1    | μA   |
| <b>TH INPUT</b>   |  |      |      |      |      |
| TH Pull-Up Current  | V <sub>CHGIN</sub> > V <sub>BAT</sub> + 100mV, Hysteresis = 50mV   | 91   | 102  | 110  | μA   |
| V <sub>TH</sub> Upper Temperature Voltage Threshold (V <sub>THH</sub> ) | Hot Detect NTC Thermistor  | 2.44 | 2.51 | 2.58 | V    |
| V <sub>TH</sub> Lower Temperature Voltage Threshold (V <sub>THL</sub> ) | Cold Detect NTC Thermistor   | 0.47 | 0.50 | 0.53 | V    |
| V <sub>TH</sub> Hysteresis  | Upper and Lower Thresholds   |      | 30   |      | mV   |

## ActivePath™ CHARGER ELECTRICAL CHARACTERISTICS CONT'D

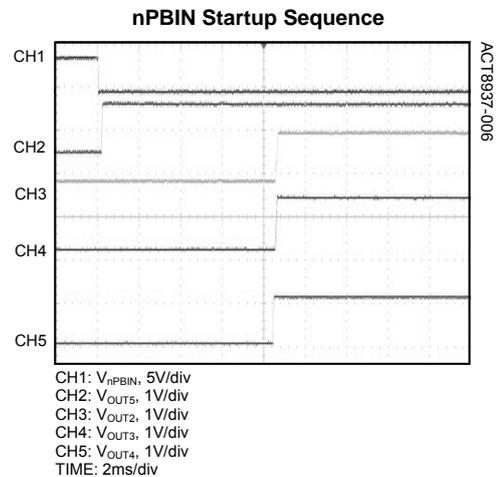
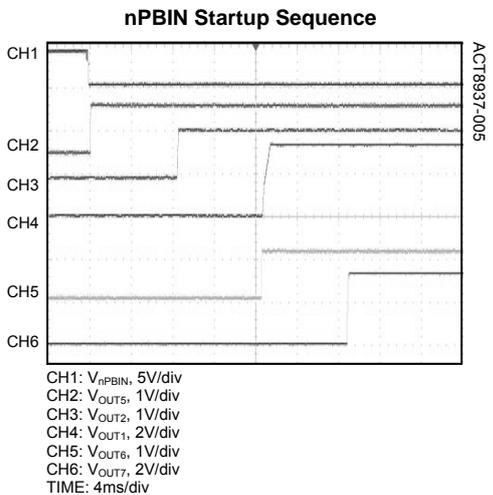
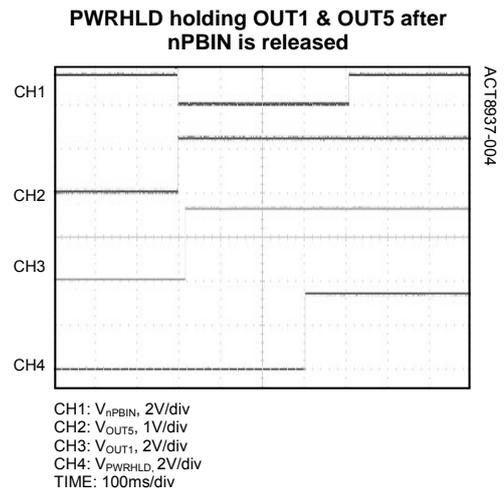
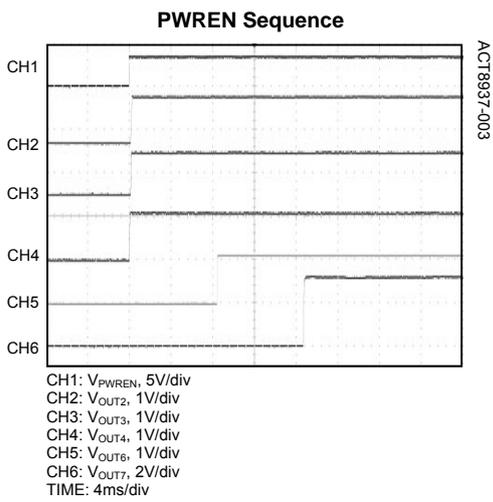
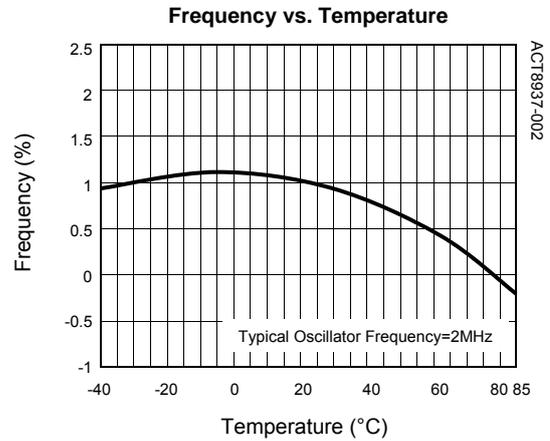
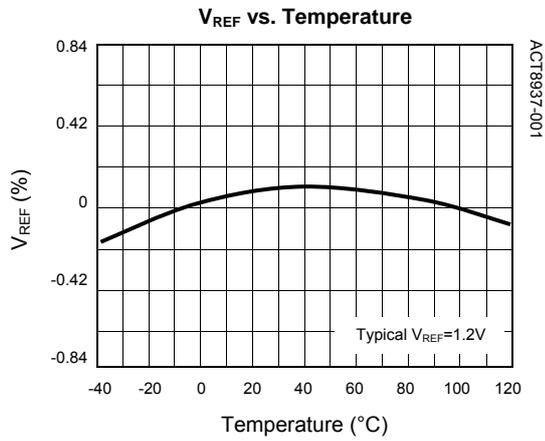
(V<sub>CHGIN</sub> = 5.0V, T<sub>A</sub> = 25°C, unless otherwise specified.)

| PARAMETER                         | TEST CONDITIONS   | MIN                        | TYP                  | MAX                           | UNIT |    |
|-----------------------------------|---|----------------------------|----------------------|-------------------------------|------|----|
| <b>CHARGER</b>                    |   |                            |                      |                               |      |    |
| BAT Reverse Leakage Current       | V <sub>CHGIN</sub> = 0V, V <sub>BAT</sub> = 4.2V, I <sub>VSYS</sub> = 0mA |                            | 8                    |                               | μA   |    |
| BAT to VSYS On-Resistance         |   |                            | 70                   |                               | mΩ   |    |
| ISET Pin Voltage                  | Fast Charge   |                            | 1.2                  |                               | V    |    |
|                                   | Precondition  |                            | 0.13                 |                               |      |    |
| Charge Termination Voltage        | T <sub>A</sub> = -20°C to 70°C  | 4.179                      | 4.2                  | 4.221                         | V    |    |
|                                   | T <sub>A</sub> = -40°C to 85°C  | 4.170                      | 4.2                  | 4.230                         |      |    |
| Charge Current                    | V <sub>BAT</sub> = 3.8V<br>R <sub>ISET</sub> = 6.8K                       | ACIN = VSYS, CHGLEV = VSYS | -10%                 | I <sub>CHG</sub> <sup>①</sup> | +10% | mA |
|                                   |   | ACIN = VSYS, CHGLEV = GA   | -10%                 | I <sub>CHG</sub> /5           | +10% |    |
|                                   |   | ACIN = GA, CHGLEV = VSYS   | 400                  | 450                           | 500  |    |
|                                   |   | ACIN = GA, CHGLEV = GA     | 80                   | 90                            | 100  |    |
| Precondition Charge Current       | V <sub>BAT</sub> = 2.7V<br>R <sub>ISET</sub> = 6.8K                       | ACIN = VSYS, CHGLEV = VSYS | 10% I <sub>CHG</sub> |                               | mA   |    |
|                                   |   | ACIN = VSYS, CHGLEV = GA   | 10% I <sub>CHG</sub> |                               |      |    |
|                                   |   | ACIN = GA, CHGLEV = VSYS   | 45                   |                               |      |    |
|                                   |   | ACIN = GA, CHGLEV = GA     | 45                   |                               |      |    |
| Precondition Threshold Voltage    | V <sub>BAT</sub> Voltage Rising   | 2.75                       | 2.85                 | 3.0                           | V    |    |
| Precondition Threshold Hysteresis | V <sub>BAT</sub> Voltage Falling  |                            | 150                  |                               | mV   |    |
| END-OF-CHARGE Current Threshold   | V <sub>BAT</sub> = 4.15V  | ACIN = VSYS, CHGLEV = VSYS | 10% I <sub>CHG</sub> |                               | mA   |    |
|                                   |   | ACIN = VSYS, CHGLEV = GA   | 10% I <sub>CHG</sub> |                               |      |    |
|                                   |   | ACIN = GA, CHGLEV = VSYS   | 45                   |                               |      |    |
|                                   |   | ACIN = GA, CHGLEV = GA     | 45                   |                               |      |    |
| Charge Restart Threshold          | V <sub>VSYS</sub> - V <sub>BAT</sub> , V <sub>BAT</sub> Falling           | 190                        | 205                  | 220                           | mV   |    |
| Precondition Safety Timer         | PRETIMO[ ] = 10   |                            | 80                   |                               | min  |    |
| Total Safety Timer                | TOTTIMO[ ] = 10   |                            | 5                    |                               | hr   |    |
| Thermal Regulation Threshold      |   |                            | 100                  |                               | °C   |    |

①: R<sub>ISET</sub> (kΩ) = 2336 × (1V/I<sub>CHG</sub> (mA)) - 0.205

## TYPICAL PERFORMANCE CHARACTERISTICS

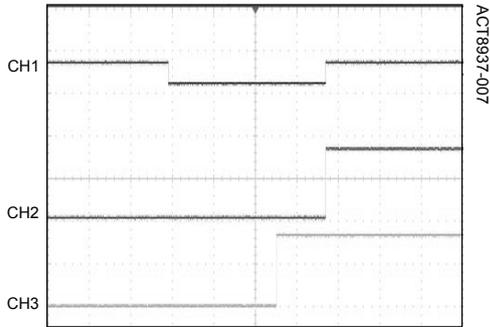
( $V_{SYS} = 3.6V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.)



## TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

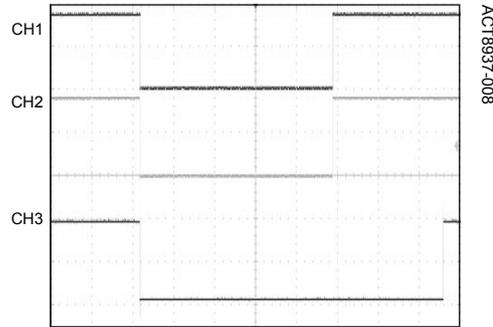
( $T_A = 25^\circ\text{C}$ , unless otherwise specified.)

Push-Button Response (First Power-Up)



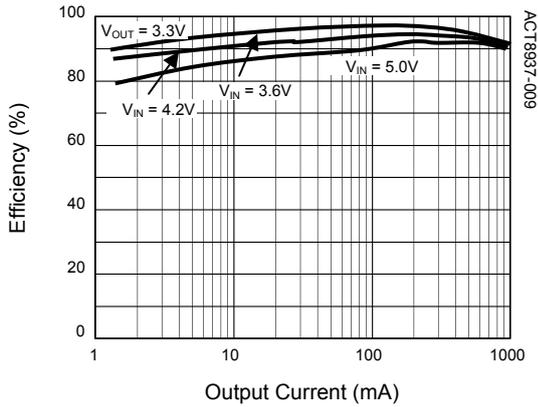
CH1:  $V_{nPBIN}$ , 2V/div  
CH2:  $V_{nPBSTAT}$ , 2V/div  
CH3:  $V_{nRSTO}$ , 2V/div  
TIME: 100ms/div  
nPBIN Resistor = 50k $\Omega$

Manual Reset Response

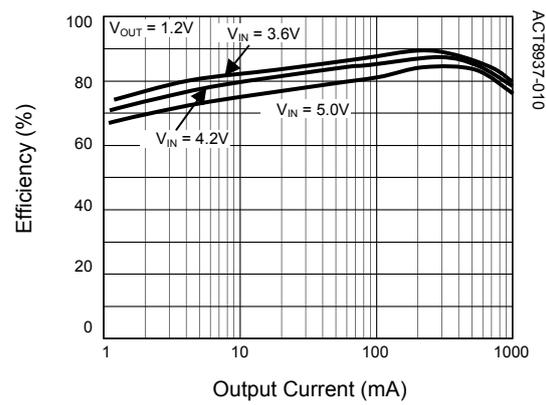


CH1:  $V_{nPBIN}$ , 2V/div  
CH2:  $V_{nPBSTAT}$ , 2V/div  
CH3:  $V_{nRSTO}$ , 2V/div  
TIME: 100ms/div  
nPBIN Resistor = 0 $\Omega$

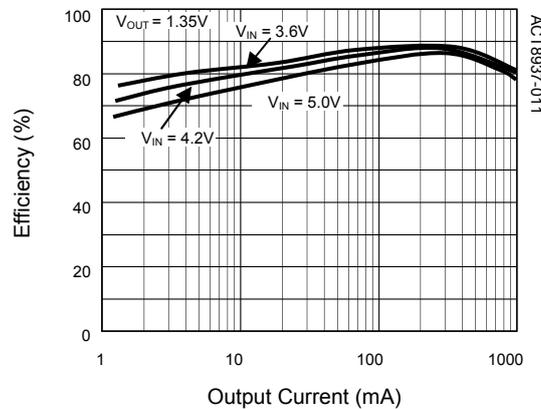
REG1 Efficiency vs. Output Current



REG2 Efficiency vs. Output Current

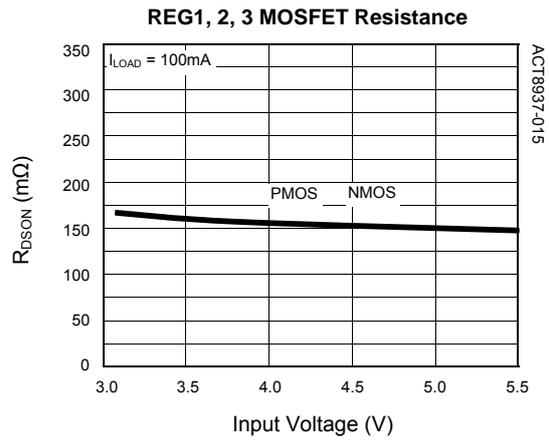
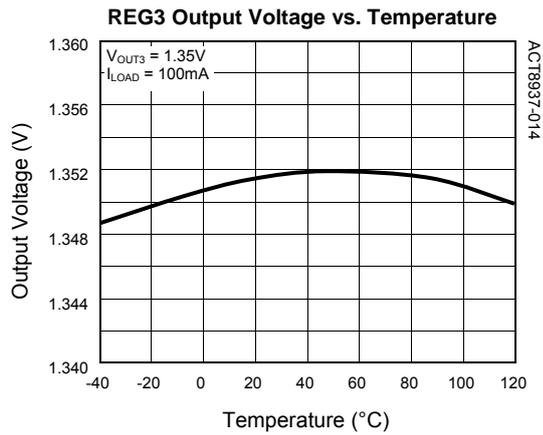
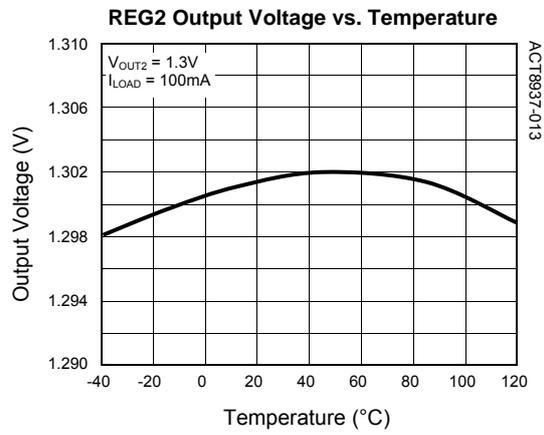
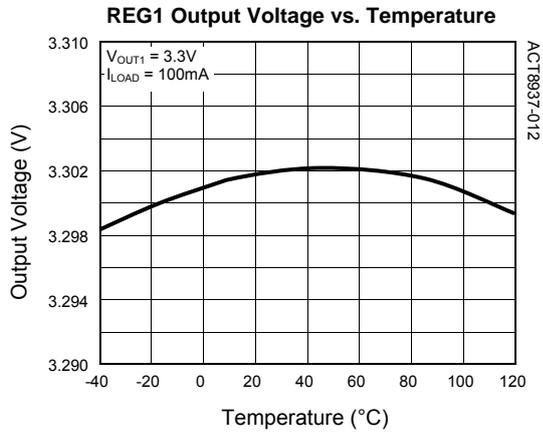


REG3 Efficiency vs. Output Current



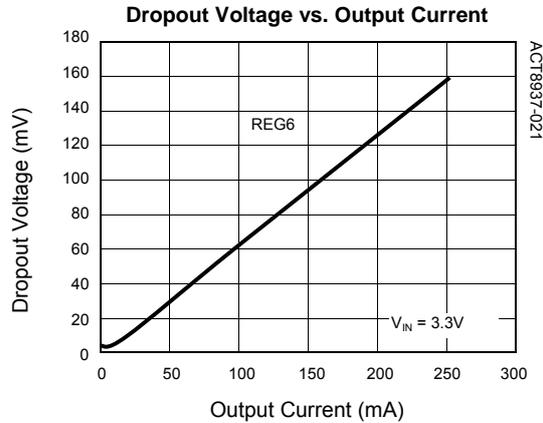
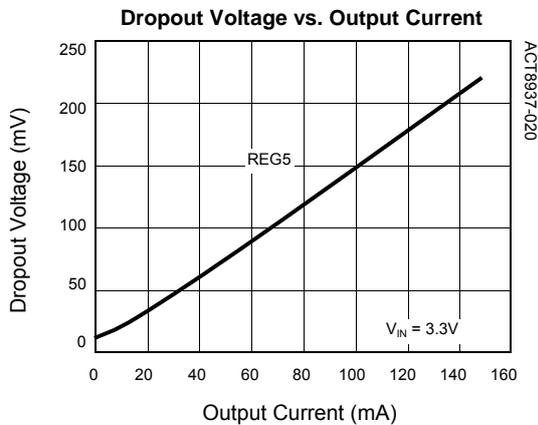
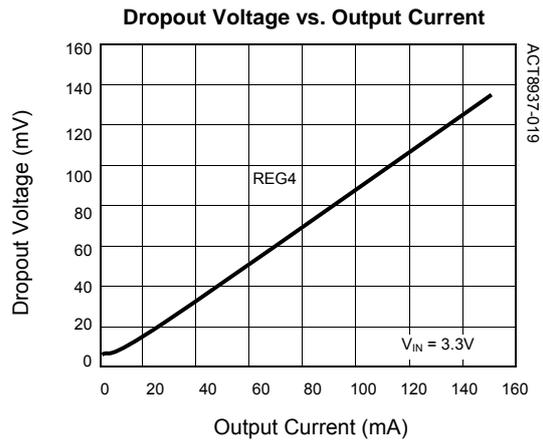
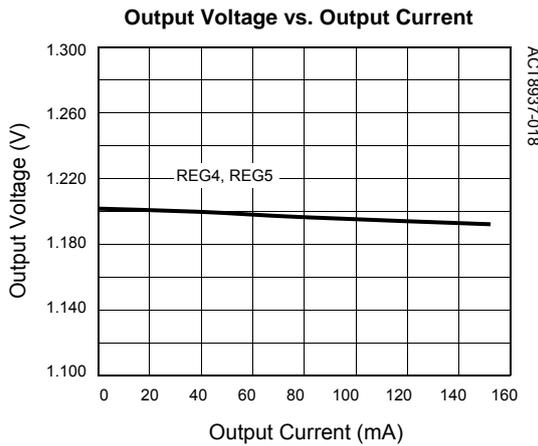
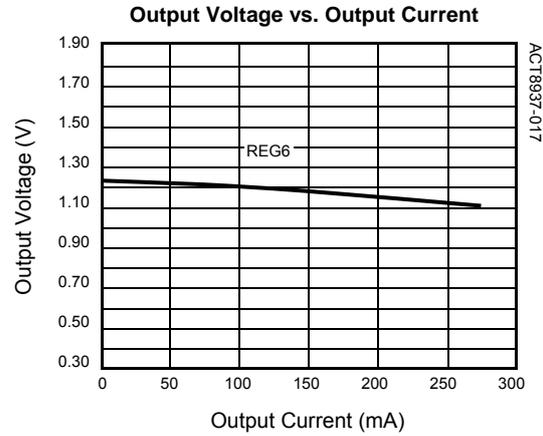
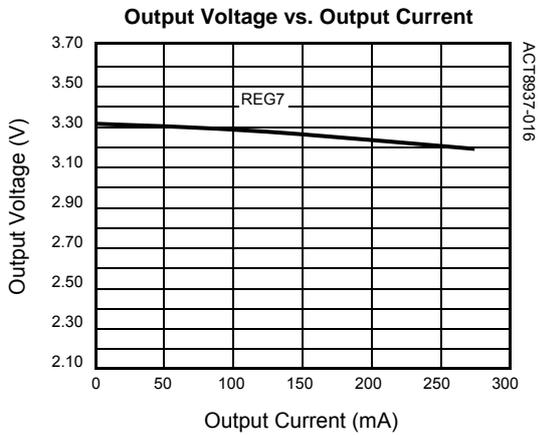
## TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

( $T_A = 25^\circ\text{C}$ , unless otherwise specified.)



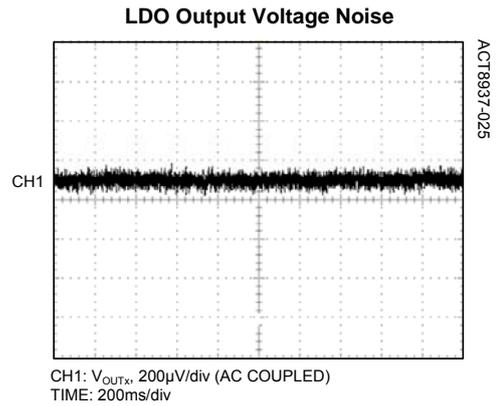
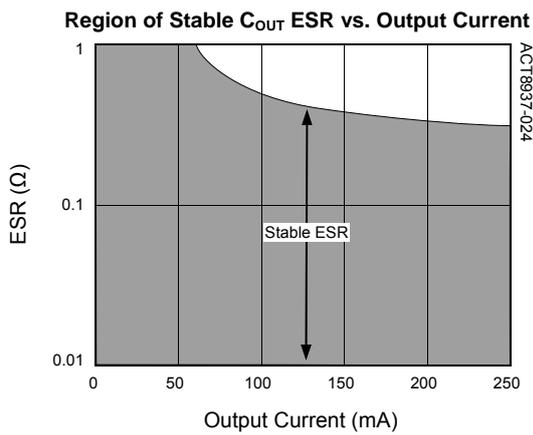
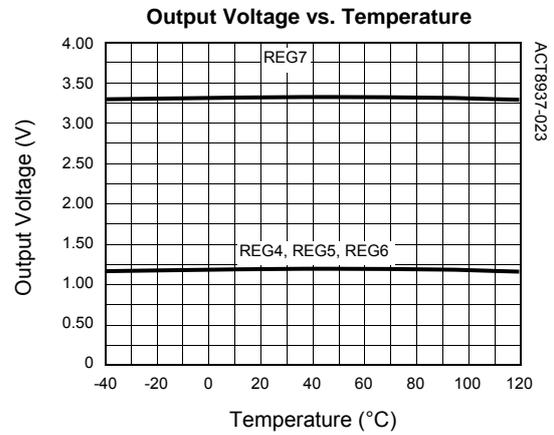
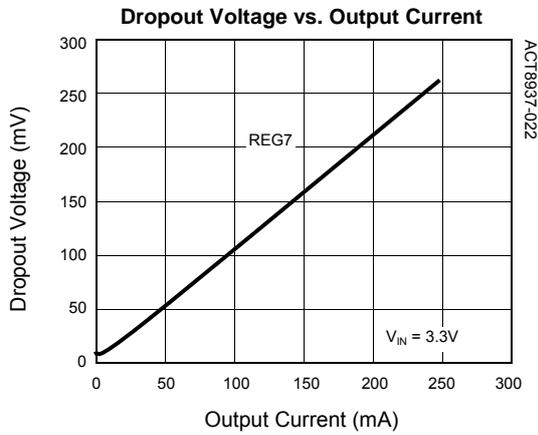
## TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

( $T_A = 25^\circ\text{C}$ , unless otherwise specified.)



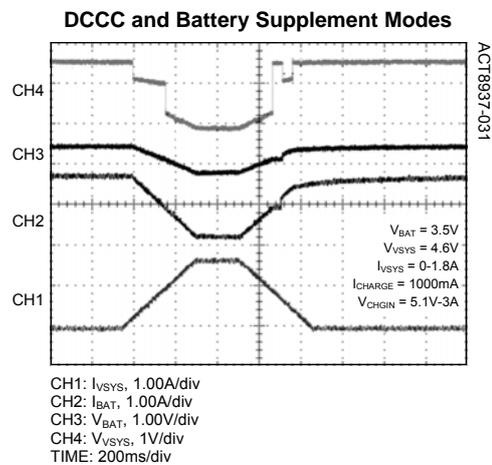
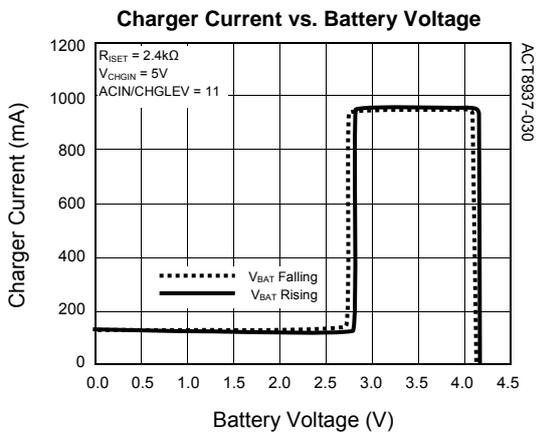
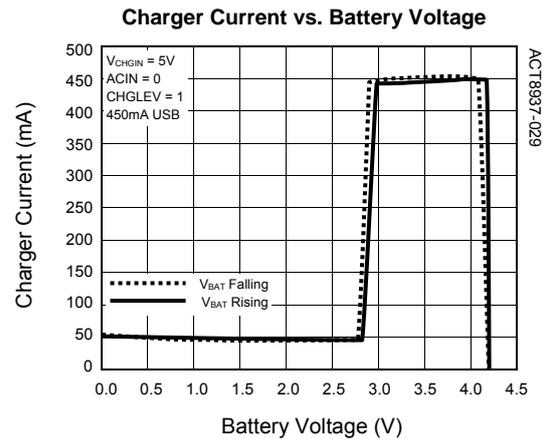
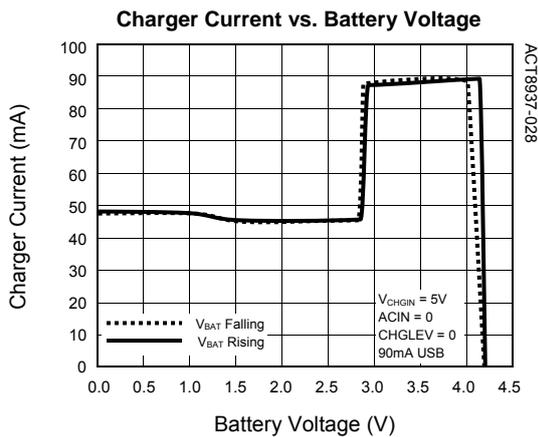
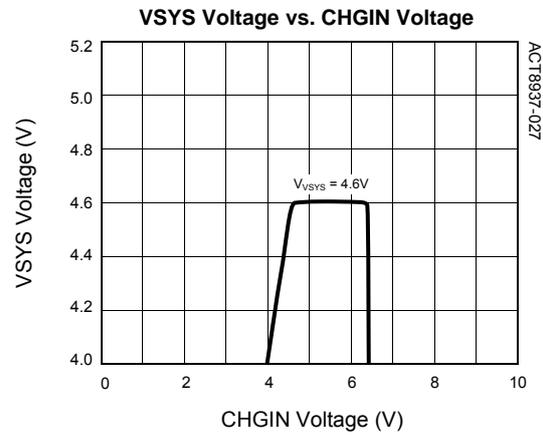
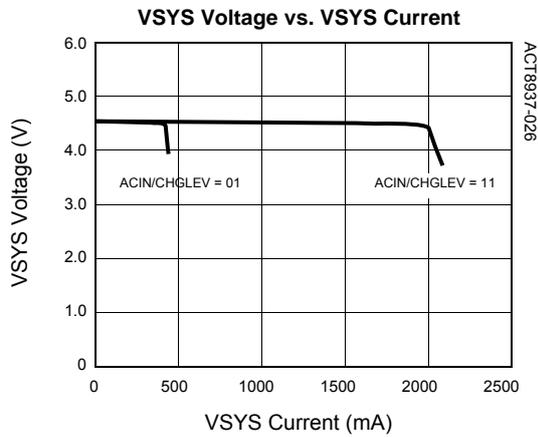
## TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

( $T_A = 25^\circ\text{C}$ , unless otherwise specified.)



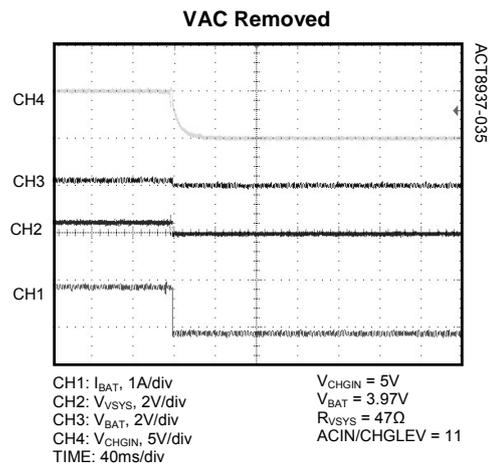
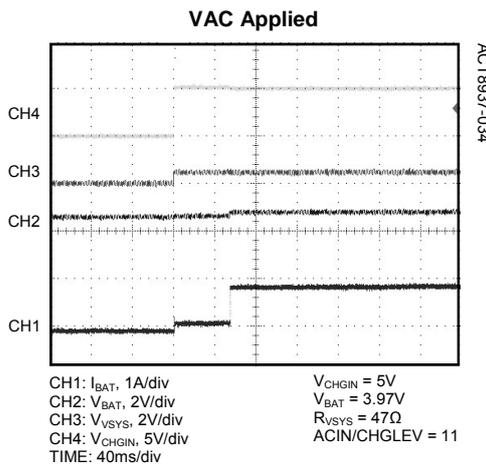
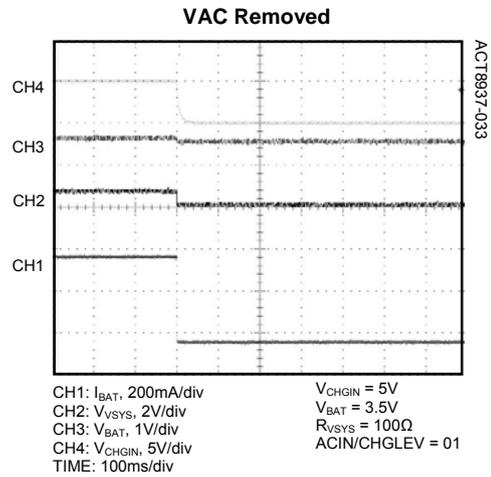
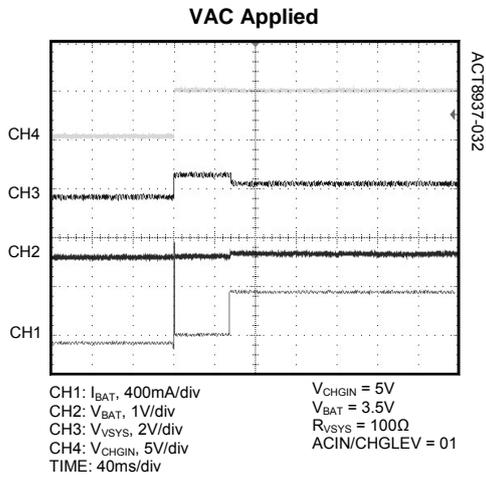
## TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

( $T_A = 25^\circ\text{C}$ , unless otherwise specified.)



## TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T<sub>A</sub> = 25°C, unless otherwise specified.)



## SYSTEM CONTROL INFORMATION

### Interfacing with the Samsung S5PC100, S5PC110 and S5PV210 Processors

The ACT8937 is optimized for use in applications using the S5PC100, S5PC110 and S5PV210 processors, supporting both the power domains as well as the signal interface for these processors.

The following paragraphs describe how to design ACT8937 with S5PV210 Processor, but the design guidelines are directly applicable to S5PC100 and S5PC110 as well.

While the ACT8937 supports many possible configurations for powering these processors, one of the most common configurations is detailed in this datasheet. In general, this document refers to the ACT8937 pin names and functions. However, in cases where the description of interconnections

between these devices benefits by doing so, both the ACT8937 pin names and the Samsung processor pin names are provided. When this is done, the S5PV210 pin names are located after the ACT8937 pin names, and are italicized and located inside parentheses. For example, PWREN (*XPWRRGTON*) refers to the logic signal applied to the ACT8937's PWREN input, identifying that it is driven from the S5PV210's XPWRRGTON output. Likewise, OUT1 (VDD\_IO) refers to ACT8937's OUT1 pin, identifying that it is connected to the S5PV210's VDD\_IO power domain.

**Table 2:**

**ACT8937 and Samsung S5PV210 Power Domains**

| POWER DOMAIN | ACT8937 CHANNEL | TYPE  | DEFAULT VOLTAGE | CURRENT CAPABILITY |
|--------------|-----------------|-------|-----------------|--------------------|
| VDD_IO       | REG1            | DC/DC | 3.3V            | 1100mA             |
| VDD_INT      | REG2            | DC/DC | 1.1V/1.1V       | 1100mA             |
| VDD_ARM      | REG3            | DC/DC | 1.25V/1.25V     | 1200mA             |
| VDD_xPLL     | REG4            | LDO   | 1.1V            | 150mA              |
| VDD_Alive    | REG5            | LDO   | 1.1V            | 150mA              |
| VDD_UOTG_D   | REG6            | LDO   | 1.1V            | 250mA              |
| VDD_UOTG_A   | REG7            | LDO   | 3.3V            | 250mA              |

**Table 3:**

**ACT8937 and Samsung S5PV210 Power Modes**

| POWER MODE | CONTROL STATE  | POWER DOMAIN STATE  | QUIESCENT CURRENT |
|------------|--|---|-------------------|
| ALL ON     | PWRHLD is asserted, PWREN is asserted  | REG1, REG2, REG3, REG4, REG5, REG6 and REG7 are all on        | 420µA             |
| NORMAL     | PWRHLD is asserted, PWREN is asserted, REG6 and REG7 are disabled after system boots up. | REG1, REG2, REG3, REG4 and REG5 are on. REG6 and REG7 are off | 340µA             |
| SLEEP      | PWRHLD is asserted, PWREN is de-asserted   | REG1 and REG5 are on. REG2, REG3, REG4, REG6 and REG7 are off | 190µA             |
| ALL OFF    | PWRHLD is de-asserted, PWREN is de-asserted  | REG1, REG2, REG3, REG4, REG5, REG6 and REG7 are all off       | <18µA             |



## nRSTO Output

nRSTO is an open-drain output which asserts low upon startup or when manual reset is asserted via the nPBIN input. When asserted on startup, nRSTO remains low until reset time-out period expires after OUT5 reaches its power-OK threshold. When asserted due to manual-reset, nRSTO immediately asserts low, then remains asserted low until the nPBIN input is de-asserted and the reset time-out period expires.

Connect a 10kΩ or greater pull-up resistor from nRSTO to an appropriate voltage supply (typically OUT1).

## nIRQ Output

nIRQ is an open-drain output that asserts low any time an interrupt is generated. Connect a 10kΩ or greater pull-up resistor from nIRQ to an appropriate voltage supply. nIRQ is typically used to drive the interrupt input of the system processor.

Many of the ACT8937's functions support interrupt-generation as a result of various conditions. These are typically masked by default, but may be unmasked via the I<sup>2</sup>C interface. For more information about the available fault conditions, refer to the appropriate sections of this datasheet.

Note that under some conditions a false interrupt may be generated upon initial startup. For this reason, it is recommended that the interrupt service routine check and validate nSYSLEVMSK[ ] and nFLTMSK[ ] bits before processing an interrupt generated by these bits. These interrupts may be validated by nSYSSTAT[ ], OK[ ] bits.

## Push-Button Control

The ACT8937 is designed to initiate a system enable sequence when the nPBIN multi-function input is asserted. Once this occurs, a power-on sequence commences, as described below. The power-on sequence must complete and the microprocessor must take control (by asserting PWREN or PWRHLD) before nPBIN is de-asserted. If the microprocessor is unable to complete its power-up routine successfully before the user releases the push-button, the ACT8937 automatically shuts the system down. This provides protection against accidental or momentary assertions of the push-button. If desired, longer "push-and-hold" times can be implemented by simply adding an additional time delay before asserting PWREN or PWRHLD.

## Control Sequences

The ACT8937 features a variety of control sequences that are optimized for supporting system enable and disable, as well as SLEEP mode of the Samsung S5PC100, S5PC110 and S5PV210 processors.

### Enabling/Disabling Sequence

A typical enable sequence is initiated whenever the following conditions occurs:

- 1) nPBIN is asserted low via 50KΩ resistance, or
- 2) A valid input voltage is present at CHGIN<sup>Ⓢ</sup>.

The enable sequence begins by enabling REG5. When REG5 reaches its power-OK threshold, nRSTO is asserted low, resetting the microprocessor. REG2, REG3 and REG4 are enabled after REG5 reaches its power-OK threshold for 8ms<sup>Ⓢ</sup>. When REG2 reaches its power-OK threshold for 8ms<sup>Ⓢ</sup>, REG1 and REG6 are enabled. When REG2 reaches its power-OK threshold for 16ms<sup>Ⓢ</sup>, REG7 is enabled. If REG5 is above its power-OK threshold when the reset timer expires, nRSTO is de-asserted, allowing the microprocessor to begin its boot sequence.

During the boot sequence, the microprocessor must assert PWRHLD, holding REG1 and REG5, and assert PWREN(XPWRRGTON), holding REG2, REG3, REG4, REG6 and REG7 to ensure that the system remains powered after nPBIN is released. REG6 and REG7 can also be enabled/disabled via I<sup>2</sup>C after microprocessor completes its boot sequence.

Once the power-up routine is completed, the system remains enabled after the push-button is released as long as either PWRHLD or PWREN are asserted high. If the processor does not assert PWRHLD before the user releases the push-button, the boot-up sequence is terminated and all regulators are disabled. This provides protection against "false-enable", when the push-button is accidentally depressed, and also ensures that the system remains enabled only if the processor successfully completes the boot-up sequence. To disable REG6 (or REG7) via I<sup>2</sup>C after the power-up, the software needs to set register bit REG6.ON[ ] (or REG7.ON[ ]) to "1" first, then set it back to "0" to turn off the regulator.

As with the enable sequence, a typical disable sequence is initiated when the user presses the push-button, which interrupts the processor via the nPBSTAT output. The actual disable sequence is completely software-controlled, but typically

①: Applicable only for ACT8937QJ2XX.

②: Typical value shown, actual delay time may vary from (T-1ms) x 88% to T x 112%, where T is the typical delay time setting.

involved initiating various “clean-up” processes before the processor finally de-asserts PWRHLD, which disables REG1 and REG5 after push-button is released. Since the processor loses power of VDD\_IO and VDD\_Alive, it automatically de-asserts PWREN (XPWRRGTON), and hence shuts the system down by disabling REG2, REG3, REG4, REG6 and REG7.

### SLEEP Mode Sequence

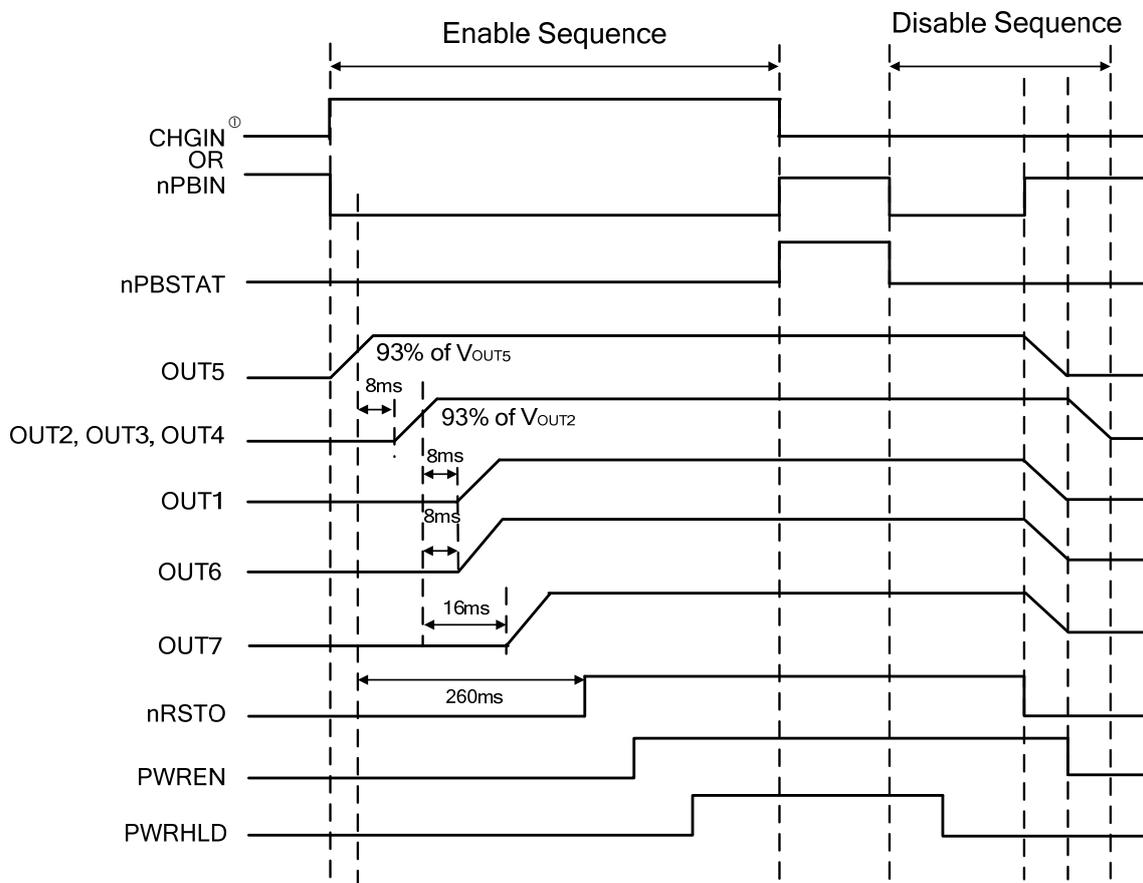
The ACT8937 supports Samsung S5PC100, S5PC110 and S5PV210 processors’ SLEEP mode operation. Once a successful power-up routine has been completed, SLEEP mode may be initiated through a variety of software-controlled mechanisms.

SLEEP mode is typically initiated when the user presses the push-button during normal operation. Pressing the push-button asserts the nPBIN input, which asserts the nPBSTAT output, which interrupts the processor. In response to this

interrupt the processor should de-assert PWREN(XPWRRGTON), disabling REG2, REG3, REG4, REG6 and REG7. PWRHLD should remain asserted during SLEEP mode so that REG1 and REG5 remain enabled.

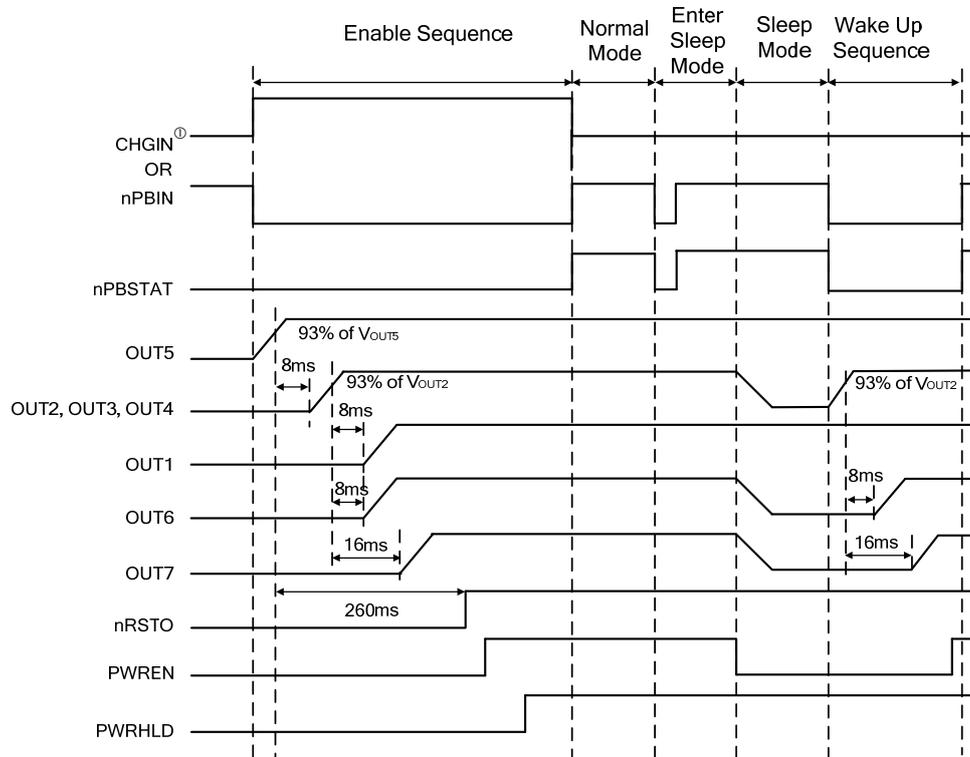
Waking up from SLEEP mode is typically initiated when the user presses the push-button again, which enables REG2, REG3, REG4, REG6 and REG7 and asserts nPBSTAT. Processors should respond by asserting PWREN(XPWRRGTON), which holds REG2, REG3, REG4, REG6 and REG7 so that normal operation may resume. An external interrupt, for instance a charger interrupt or a RTC interrupt, can also initiate a wake up sequence. When an external interrupt is sent to the processor, the processor should response by getting itself ready to wake up from SLEEP mode first, then assert PWREN(XPWRRGTON), which enables REG2, REG3, REG4, REG6 and REG7 so that the normal operation may resume.

**Figure 3:**  
**Enable/Disable Sequence**

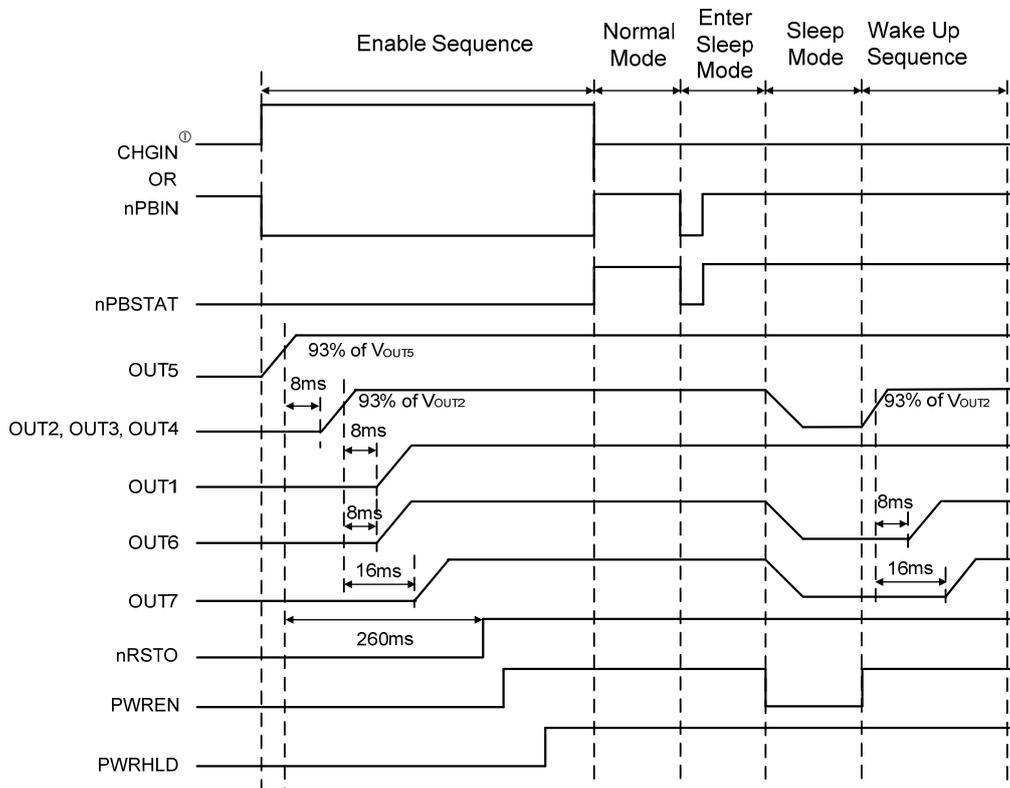


①: Applicable only for ACT8937QJ2XX.

**Figure 4:**  
**Sleep Mode and Wake up Sequence (from Push-Button)**



**Figure 5:**  
**Sleep Mode and Wake up Sequence (from External Interrupt)**



①: Applicable only for ACT8937QJ2XX.

## FUNCTIONAL DESCRIPTION

### I<sup>2</sup>C Interface

The ACT8937 features an I<sup>2</sup>C interface that allows advanced programming capability to enhance overall system performance. To ensure compatibility with a wide range of system processors, the I<sup>2</sup>C interface supports clock speeds of up to 400kHz (“Fast-Mode” operation) and uses standard I<sup>2</sup>C commands. I<sup>2</sup>C write-byte commands are used to program the ACT8937, and I<sup>2</sup>C read-byte commands are used to read the ACT8937’s internal registers. The ACT8937 always operates as a slave device, and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation, [1011011x].

SDA is a bi-directional data line and SCL is a clock input. The master device initiates a transaction by issuing a START condition, defined by SDA transitioning from high to low while SCL is high. Data is transferred in 8-bit packets, beginning with the MSB, and is clocked-in on the rising edge of SCL. Each packet of data is followed by an “Acknowledge” (ACK) bit, used to confirm that the data was transmitted successfully.

For more information regarding the I<sup>2</sup>C 2-wire serial interface, go to the NXP website: <http://www.nxp.com>.

### Voltage Monitor and Interrupt

#### Programmable System Voltage Monitor

The ACT8937 features a programmable system-voltage monitor, which monitors the voltage at VSYS and compares it to a programmable threshold voltage. The programmable voltage threshold is programmed by SYSLEV[3:0], as shown in Table 6.

SYSLEV[ ] is set to 3.0V by default. There is a 200mV rising hysteresis on SYSLEV[ ] threshold such that V<sub>VSYS</sub> needs to be 3.2V(typ) or higher in order to power up the IC.

The nSYSSTAT[ ] bit reflects the output of an internal voltage comparator that monitors V<sub>VSYS</sub> relative to the SYSLEV[ ] voltage threshold, the value of nSYSSTAT[ ] = 1 when V<sub>VSYS</sub> is lower than the SYSLEV[ ] voltage threshold, and nSYSSTAT[ ] = 0 when V<sub>VSYS</sub> is higher than the SYSLEV[ ] voltage threshold. Note that the SYSLEV[ ] voltage threshold is defined for falling voltages, and that the comparator produces about 200mV of hysteresis at VSYS. As a result, once V<sub>VSYS</sub> falls below the SYSLEV threshold, its voltage must increase by more than about 200mV to clear that condition.

After the IC is powered up, the ACT8937 responds in one of two ways when the voltage at VSYS falls below the SYSLEV[ ] voltage threshold:

1) If nSYSMODE[ ] = 1 (default case), when system voltage level interrupt is unmasked (nSYSLEVMSK[ ]=1) and V<sub>VSYS</sub> falls below the programmable threshold, the ACT8937 asserts nIRQ, providing a software “under-voltage alarm”. The response to this interrupt is controlled by the CPU, but will typically initiate a controlled shutdown sequence either or alert the user that the battery is low. In this case the interrupt is cleared when V<sub>VSYS</sub> rises up again above the SYSLEV rising threshold and nSYSSTAT[ ] is read via I<sup>2</sup>C.

2) If nSYSMODE[ ] = 0, when V<sub>VSYS</sub> falls below the programmable threshold the ACT8937 shuts down, immediately disabling all regulators. This option is useful for implementing a programmable “under-voltage lockout” function that forces the system off when the battery voltage falls below the SYSLEV threshold voltage. Since this option does not support a controlled shutdown sequence, it is generally used as a “fail-safe” to shut the system down when the battery voltage is too low.

**Table 6:**

**SYSLEV Falling Threshold**

| SYSLEV[3:0] | SYSLEV Falling Threshold<br>(Hysteresis = 200mV) |
|-------------|--|
| 0000        | 2.3  |
| 0001        | 2.4  |
| 0010        | 2.5  |
| 0011        | 2.6  |
| 0100        | 2.7  |
| 0101        | 2.8  |
| 0110        | 2.9  |
| 0111        | 3.0  |
| 1000        | 3.1  |
| 1001        | 3.2  |
| 1010        | 3.3  |
| 1011        | 3.4  |
| 1100        | 3.5  |
| 1101        | 3.6  |
| 1110        | 3.7  |
| 1111        | 3.8  |

#### Precision Voltage Detector

The LBI input connects to one input of a precision voltage comparator, which can be used to monitor a system voltage such as the battery voltage. An external resistive-divider network can be used to set voltage monitoring thresholds, as shown in *Functional Block Diagram*. The output of the comparator is present at the nLBO open-drain output.

## Thermal Shutdown

The ACT8937 integrates thermal shutdown protection circuitry to prevent damage resulting from excessive thermal stress, as may be encountered under fault conditions. This circuitry disables all regulators if the ACT8937 die temperature exceeds 160°C, and prevents the regulators from being enabled until the IC temperature drops by 20°C (typ).

## STEP-DOWN DC/DC REGULATORS

### General Description

The ACT8937 features three synchronous, fixed-frequency, current-mode PWM step down converters that achieve peak efficiencies of up to 97%. REG1 and REG2 are capable of supplying up to 1100mA of output current, while REG3 supports up to 1200mA. These regulators operate with a fixed frequency of 2MHz, minimizing noise in sensitive applications and allowing the use of small external components.

### 100% Duty Cycle Operation

Each regulator is capable of operating at up to 100% duty cycle. During 100% duty-cycle operation, the high-side power MOSFET is held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery powered applications.

### Synchronous Rectification

REG1, REG2, and REG3 each feature integrated n-channel synchronous rectifiers, maximizing efficiency and minimizing the total solution size and cost by eliminating the need for external rectifiers.

### Soft-Start

When enabled, each output voltages tracks an internal 400 $\mu$ s soft-start ramp, minimizing input current during startup and allowing each regulator to power up in a smooth, monotonic manner that is independent of output load conditions.

### Compensation

Each buck regulator utilizes current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over its full operating range. No compensation design is required; simply follow a few simple guidelines described below when choosing external components.

#### *Input Capacitor Selection*

The input capacitor reduces peak currents and noise induced upon the voltage source. A 4.7 $\mu$ F ceramic capacitor is recommended for each regulator in most applications.

#### *Output Capacitor Selection*

For most applications, 22 $\mu$ F ceramic output capacitors are recommended for REG1, REG2 and REG3.

Despite the advantages of ceramic capacitors, care

must be taken during the design process to ensure stable operation over the full operating voltage and temperature range. Ceramic capacitors are available in a variety of dielectrics, each of which exhibits different characteristics that can greatly affect performance over their temperature and voltage ranges.

Two of the most common dielectrics are Y5V and X5R. Whereas Y5V dielectrics are inexpensive and can provide high capacitance in small packages, their capacitance varies greatly over their voltage and temperature ranges and are not recommended for DC/DC applications. X5R and X7R dielectrics are more suitable for output capacitor applications, as their characteristics are more stable over their operating ranges, and are highly recommended.

#### *Inductor Selection*

REG1, REG2, and REG3 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. These devices were optimized for operation with 2.2 $\mu$ H inductors, although inductors in the 1.5 $\mu$ H to 3.3 $\mu$ H range can be used. Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current by at least 30%.

### Configuration Options

#### *Output Voltage Programming*

By default, each regulator powers up and regulates to its default output voltage. Output voltage is selectable by setting VSEL pin that when VSEL is low, output voltage is programmed by VSET1[ ] bits, and when VSEL is high, output voltage is programmed by VSET2[ ] bits. However, once the system is enabled, each regulator's output voltage may be independently programmed to a different value, typically in order to minimize the power consumption of the microprocessor during some operating modes. Program the output voltages via the I<sup>2</sup>C serial interface by writing to the regulator's VSET1[ ] register if VSEL is low or VSET2[ ] register if VSEL is high as shown in Table 8.

#### *Enable / Disable Control*

During normal operation, each buck may be enabled or disabled via the I<sup>2</sup>C interface by writing to that regulator's ON[ ] bit. The regulator accept rising or falling edge of ON[ ] bit as on/off signal. To enable the regulator, clear ON[ ] to 0 first then set to 1. To disable the regulator, set ON[ ] to 1 first then clear it to 0.

### REG1, REG2, REG3 Turn-on Delay

Each of REG1, REG2 and REG3 features a programmable Turn-on Delay which help ensure a reliable qualification. This delay is programmed by DELAY[2:0], as shown in Table 7.

**Table 7:**

**REGx/DELAY[ ] Turn-On Delay**

| DELAY[2] | DELAY[1] | DELAY[0] | TURN-ON DELAY |
|----------|----------|----------|---------------|
| 0        | 0        | 0        | 0 ms          |
| 0        | 0        | 1        | 2 ms          |
| 0        | 1        | 0        | 4 ms          |
| 0        | 1        | 1        | 8 ms          |
| 1        | 0        | 0        | 16 ms         |
| 1        | 0        | 1        | 32 ms         |
| 1        | 1        | 0        | 64 ms         |
| 1        | 1        | 1        | 128 ms        |

### Operating Mode

By default, REG1, REG2, and REG3 each operate in fixed-frequency PWM mode at medium to heavy loads, while automatically transitioning to a proprietary power-saving mode at light loads in order to maximize standby battery life. In applications where low noise is critical, force fixed-frequency PWM operation across the entire load current range, at the expense of light-load efficiency, by setting the MODE[ ] bit to 1.

### OK[ ] and Output Fault Interrupt

Each DC/DC features a power-OK status bit that can be read by the system microprocessor via the I<sup>2</sup>C interface. If an output voltage is lower than the power-OK threshold, typically 7% below the programmed regulation voltage, that regulator's OK[ ] bit will be 0.

If a DC/DC's nFLTMSK[ ] bit is set to 1, the ACT8937 will interrupt the processor if that DC/DC's output voltage falls below the power-OK threshold. In this case, nIRQ will assert low and remain asserted until either the regulator is turned off or back in regulation, and the OK[ ] bit has been read via I<sup>2</sup>C.

### PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors.

Step-down DC/DCs exhibit discontinuous input current, so the input capacitors should be placed as close as possible to the IC, and avoiding the use of via if possible. The inductor, input filter capacitor, and output filter capacitor should be connected as close together as possible, with short, direct, and wide traces. The ground nodes for each regulator's power loop should be connected at a single point in a star-ground configuration, and this point should be connected to the backside ground plane with multiple via. The output node for each regulator should be connected to its corresponding OUTx pin through the shortest possible route, while keeping sufficient distance from switching nodes to prevent noise injection. Finally, the exposed pad should be directly connected to the backside ground plane using multiple via to achieve low electrical and thermal resistance.

**Table 8:**

**REGx/VSET[ ] Output Voltage Setting**

| REGx/VSET[2:0] | REGx/VSET[5:3] |       |       |       |       |       |       |       |
|----------------|----------------|-------|-------|-------|-------|-------|-------|-------|
|                | 000            | 001   | 010   | 011   | 100   | 101   | 110   | 111   |
| 000            | 0.600          | 0.800 | 1.000 | 1.200 | 1.600 | 2.000 | 2.400 | 3.200 |
| 001            | 0.625          | 0.825 | 1.025 | 1.250 | 1.650 | 2.050 | 2.500 | 3.300 |
| 010            | 0.650          | 0.850 | 1.050 | 1.300 | 1.700 | 2.100 | 2.600 | 3.400 |
| 011            | 0.675          | 0.875 | 1.075 | 1.350 | 1.750 | 2.150 | 2.700 | 3.500 |
| 100            | 0.700          | 0.900 | 1.100 | 1.400 | 1.800 | 2.200 | 2.800 | 3.600 |
| 101            | 0.725          | 0.925 | 1.125 | 1.450 | 1.850 | 2.250 | 2.900 | 3.700 |
| 110            | 0.750          | 0.950 | 1.150 | 1.500 | 1.900 | 2.300 | 3.000 | 3.800 |
| 111            | 0.775          | 0.975 | 1.175 | 1.550 | 1.950 | 2.350 | 3.100 | 3.900 |

## LOW-NOISE, LOW-DROPOUT LINEAR REGULATORS

### General Description

REG4, REG5, REG6, and REG7 are low-noise, low-dropout linear regulators (LDOs) that supply up to 150mA, 150mA, 250mA, and 250mA, respectively. Each LDO has been optimized to achieve low noise and high-PSRR, achieving more than 65dB PSRR at frequencies up to 10kHz.

### Output Current Limit

Each LDO contains current-limit circuitry featuring a current-limit fold-back function. During normal and moderate overload conditions, the regulators can support more than their rated output currents. During extreme overload conditions, however, the current limit is reduced by approximately 30%, reducing power dissipation within the IC.

### Compensation

The LDOs are internally compensated and require very little design effort, simply select input and output capacitors according to the guidelines below.

#### *Input Capacitor Selection*

Each LDO requires a small ceramic input capacitor to supply current to support fast transients at the input of the LDO. Bypassing each INL pin to GA with 1 $\mu$ F. High quality ceramic capacitors such as X7R and X5R dielectric types are strongly recommended.

#### *Output Capacitor Selection*

Each LDO requires a small ceramic output capacitor for stability. Capacitance value is 1.5 $\mu$ F for REG4 and REG5, 2.2 $\mu$ F for REG6 and REG7. For best performance, each output capacitor should be connected directly between the output and GA pins, as close to the output as possible, and with a short, direct connection. High quality ceramic capacitors such as X7R and X5R dielectric types are strongly recommended.

### Configuration Options

#### *Output Voltage Programming*

By default, each LDO powers up and regulates to its default output voltage. Once the system is enabled, each output voltage may be independently programmed to a different value by writing to the regulator's VSET[ ] register via the I<sup>2</sup>C serial interface as shown in Table 8.

#### *Enable / Disable Control*

During normal operation, each LDO may be enabled or disabled via the I<sup>2</sup>C interface by writing

to that LDO's ON[ ] bit. The regulator accept rising or falling edge of ON[ ] bit as on/off signal. To enable the regulator, clear ON[ ] to 0 first then set to 1. To disable the regulator, set ON[ ] to 1 first then clear it to 0.

#### *REG4, REG5, REG6, REG7 Turn-on Delay*

Each of REG4, REG5, REG6 and REG7 features a programmable Turn-on Delay which help ensure a reliable qualification. This delay is programmed by DELAY[2:0], as shown in Table 7.

#### *Output Discharge*

Each of the ACT8937's LDOs features an optional output discharge function, which discharges the output to ground through a 1.5k $\Omega$  resistance when the LDO is disabled. This feature may be enabled or disabled by setting DIS[ ]; set DIS[ ] to 1 to enable this function, clear DIS[ ] to 0 to disable it.

#### *Low-Power Mode*

Each of ACT8937's LDOs features a LOWIQ[ ] bit which, when set to 1, reduces the LDO's quiescent current by about 16%, saving power and extending battery lifetime.

### OK[ ] and Output Fault Interrupt

Each LDO features a power-OK status bit that can be read by the system microprocessor via the interface. If an output voltage is lower than the power-OK threshold, typically 11% below the programmed regulation voltage, the value of that regulator's OK[ ] bit will be 0.

If a LDO's nFLTMSK[ ] bit is set to 1, the ACT8937 will interrupt the processor if that LDO's output voltage falls below the power-OK threshold. In this case, nIRQ will assert low and remain asserted until either the regulator is turned off or back in regulation, and the OK[ ] bit has been read via I<sup>2</sup>C.

### PCB Layout Considerations

The ACT8937's LDOs provide good DC, AC, and noise performance over a wide range of operating conditions, and are relatively insensitive to layout considerations. When designing a PCB, however, careful layout is necessary to prevent other circuitry from degrading LDO performance.

A good design places input and output capacitors as close to the LDO inputs and output as possible, and utilizes a star-ground configuration for all regulators to prevent noise-coupling through ground. Output traces should be routed to avoid close proximity to noisy nodes, particularly the SW

nodes of the DC/DCs.

REFBP is a noise-filtered reference, and internally has a direct connection to the linear regulator controller. Any noise injected into REFBP will directly affect the outputs of the linear regulators, and therefore special care should be taken to ensure that no noise is injected to the outputs via REFBP. As with the LDO output capacitors, the REFBP bypass capacitor should be placed as close to the IC as possible, with short, direct connections to the star-ground. Avoid the use of via whenever possible. Noisy nodes, such as from the DC/DCs, should be routed as far away from REFBP as possible.

## ActivePath™ CHARGER

### General Description

The ACT8937 features an advanced battery charger that incorporates the patent-pending *ActivePath architecture for system power selection*. This combination of circuits provides a complete, advanced battery-management system that automatically selects the best available input supply, manages charge current to ensure system power availability, and provides a complete, high-accuracy ( $\pm 0.5\%$ ), thermally regulated, full-featured single-cell linear Li+ charger that can withstand input voltages of up to 12V.

### ActivePath Architecture

The *ActivePath* architecture performs three important functions:

- 1) System Configuration Optimization
- 2) Input Protection
- 3) Battery-Management

### System Configuration Optimization

The *ActivePath* circuitry monitors the state of the input supply, the battery, and the system, and automatically reconfigures itself to optimize the power system. If a valid input supply is present, *ActivePath* powers the system from the input while charging the battery in parallel. This allows the battery to charge as quickly as possible, while supplying the system. If a valid input supply is not present, *ActivePath* powers the system from the battery. Finally, if the input is present and the system current requirement exceeds the capability of the input supply, *ActivePath* allows system power to be drawn from both the battery and the input supply.

### Input Protection

#### Input Over-Voltage Protection

The *ActivePath* circuitry features input over-voltage protection circuitry. This circuitry disables charging when the input voltage exceeds the voltage set by OVPSET[ ] as shown in Table 9, but stands off the input voltage in order to protect the system. Note that the adjustable OVP threshold is intended to provide the charge cycle with adjustable immunity against upward voltage transients on the input, and is not intended to allow continuous charging with input voltages above the charger's normal operating voltage range. Independent of the OVPSET[ ] setting, the charge cycle is not allowed to resume until the input voltage falls back into the charger's normal operating voltage range (i.e. below 6.0V).

In an input over-voltage condition this circuit limits  $V_{VSYS}$  to 4.6V, protecting any circuitry connected to VSYS from the over-voltage condition, which may exceed this circuitry's voltage capability. This circuit is capable of withstanding input voltages of up to 12V.

Table 9:

Input Over-Voltage Protection Setting

| OVPSET[1] | OVPSET[0] | OVP THRESHOLD |
|-----------|-----------|---------------|
| 0         | 0         | 6.6V          |
| 0         | 1         | 7.0V          |
| 1         | 0         | 7.5V          |
| 1         | 1         | 8.0V          |

#### Input Supply Overload Protection

The *ActivePath* circuitry monitors and limits the total current drawn from the input supply to a value set by the ACIN and CHGLEV inputs, as well as the resistor connected to ISET. Drive ACIN to a logic-low for "USB Mode", which limits the input current to either 100mA, when CHGLEV is driven to a logic-low, or 450mA, when CHGLEV is driven to a logic-high. Drive ACIN to a logic-high for "AC-Mode", which limits the input current to 2A, typically.

#### Input Under Voltage Lockout

If the input voltage applied to CHGIN falls below 3.5V (typ), an input under-voltage condition is detected and the charger is disabled. Once an input under-voltage condition is detected, a new charge cycle will initiate when the input exceeds the under-voltage threshold by at least 500mV.

### Battery Management

The ACT8937 features a full-featured, intelligent charger for Lithium-based cells, and was designed specifically to provide a complete charging solution with minimum system design effort.

The core of the charger is a CC/CV (Constant-Current/Constant-Voltage), linear-mode charge controller. This controller incorporates current and voltage sense circuitry, an internal 70m $\Omega$  power MOSFET, thermal-regulation circuitry, a full-featured state machine that implements charge control and safety features, and circuitry that eliminates the reverse blocking diode required by conventional charger designs.

The charge termination voltage is highly accurate ( $\pm 0.5\%$ ), and features a selection of charge safety time-out periods that protect the system from operation with damaged cells. Other features include pin-programmable fast-charge current and

one current-limited nSTAT output that can directly drive LED indicator or provide a logic-level status signal to the host microprocessor.

### Dynamic Charge Current Control (DCCC)

The ACT8937's *ActivePath* charger features dynamic charge current control (DCCC) circuitry, which acts to ensure that the system remains powered while operating within the maximum output capability of the power adapter. The DCCC circuitry continuously monitors  $V_{VSYS}$ , and if the voltage at VSYS drops by more than 200mV, the DCCC circuitry automatically reduces charge current in order to prevent  $V_{VSYS}$  from continuing to drop.

### Charge Current Programming

The ACT8937's *ActivePath* charger features a flexible charge current-programming scheme that combines the convenience of internal charge current programming with the flexibility of resistor based charge current programming. Current limits and charge current programming are managed as a function of the ACIN and CHGLEV pins, in combination with  $R_{ISET}$ , the resistance connected to the ISET pin.

ACIN is a logic input that configures the current-limit of *ActivePath*'s linear regulator as well as that of the battery charger. ACIN features a precise 1.2V logic threshold, so that the input voltage detection threshold may be adjusted with a simple resistive voltage divider. This input also allows a simple, low-cost dual-input charger switch to be implemented with just a few, low-cost components.

When the voltage at ACIN is above the 1.2V threshold, the charger operates in "AC-Mode" with a charge current programmed by  $R_{ISET}$ , and the  $R_{ISET}$  is given by:

$$R_{ISET} \text{ (k}\Omega\text{)} = 2336 \times (1V/I_{CHG} \text{ (mA)}) - 0.205$$

With a given  $R_{ISET}$  then charge current will reduce 5 times when CHGLEV is driven low.

When ACIN is below the 1.2V threshold, the charger operates in "USB-Mode", with a maximum CHGIN input current and charge current defined by the CHGLEV input; 450mA, if CHGLEV is driven to a logic-high, or 100mA, if CHGLEV is driven to a

logic-low.

The ACT8937's charge current settings are summarized in Table 10.

Note that the actual charge current may be limited to a current lower than the programmed fast charge current due to the ACT8937's internal thermal regulation loop. See the *Thermal Regulation* section for more information.

### Charger Input Interrupts

In order to ease input supply detection and eliminate the size and cost of external detection circuitry, the charger has the ability to generate interrupts based upon the status of the input supply. This function is capable of generating an interrupt when the input is connected, disconnected, or both. An interrupt is generated any time the input supply is connected when INSTAT[ ] bit is set to 1 and the INCON[ ] bit is set to 1, and an interrupt is generated any time the input supply is disconnected when INSTAT[ ] bit is set to 1 and the INDIS[ ] bit is set to 1.

INDAT[ ] indicates the status of the CHGIN input supply. A value of 1 indicates that a valid CHGIN input ( $CHGIN \text{ UVLO Threshold} < V_{CHGIN} < CHGIN \text{ OVP Threshold}$ ) is present, a value of 0 indicates a valid input is not present.

When an interrupt is generated by the input supply, reading the INSTAT[ ] returns a value of 1. INSTAT [ ] is automatically cleared to 0 upon reading. When no interrupt is generated by the input supply, reading the INSTAT[ ] returns a value of 0.

When responding to an Input Status Interrupt, it is often useful to know the state of the ACIN input. For example, in a dual-input charger application knowing the state of the ACIN input can identify which type of input supply has been connected. The state of the ACIN input can be read at any time by reading the ACINSTAT[ ] bit, where a value of 1 indicates that the voltage at ACIN is above the 1.2V threshold (indicating that a wall-cube has been attached), and a value of 0 indicates that the voltage is below this threshold (indicating that ACIN input is not valid and USB supply input is selected).

Table 10:

ACIN and CHGLEV Inputs

| ACIN | CHGLEV | CHARGE CURRENT (mA) | PRECONDITION CHARGE CURRENT (mA) |
|------|--------|---------------------|----------------------------------|
| 0    | 0      | 90                  | 45                               |
| 0    | 1      | 450                 | 45                               |
| 1    | 0      | $I_{CHG}/5$         | $10\% \times I_{CHG}$            |
| 1    | 1      | $I_{CHG}$           | $10\% \times I_{CHG}$            |

Figure 6:  
Typical Li+ charge profile and ACT8937 charge states

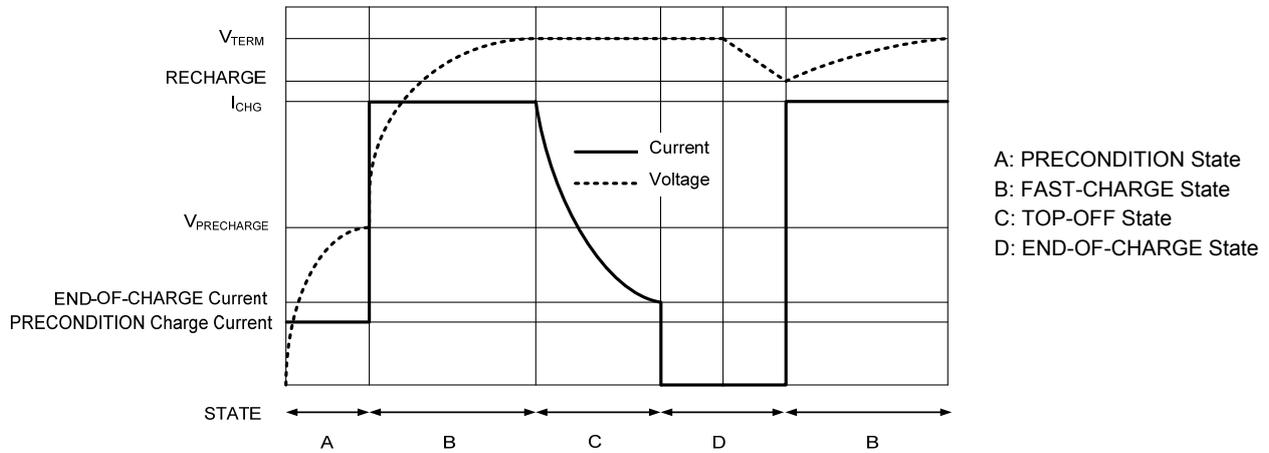
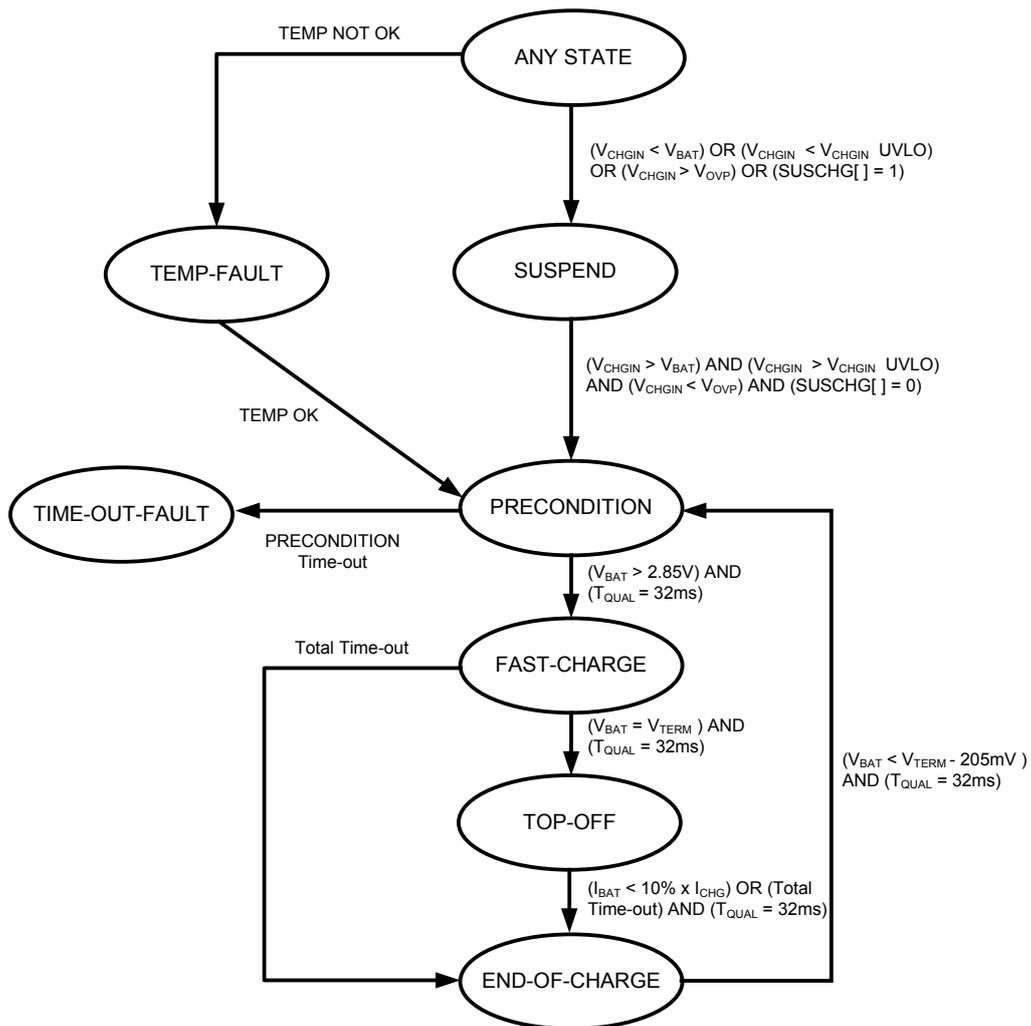


Figure 7:  
Charger State Diagram



## Charge-Control State Machine

### PRECONDITION State

A new charging cycle begins with the PRECONDITION state, and operation continues in this state until  $V_{BAT}$  exceeds the Precondition Threshold Voltage. When operating in PRECONDITION state, the cell is charged at 10% of the programmed maximum fast-charge constant current,  $I_{CHG}$ .

Once  $V_{BAT}$  reaches the Precondition Threshold Voltage, the state machine jumps to the FAST-CHARGE state. If  $V_{BAT}$  does not reach the Precondition Threshold Voltage before the Precondition Time-out period expires, then the state machine jumps to the TIME-OUT-FAULT state in order to prevent charging a damaged cell. See the *Charge Safety Timers* section for more information.

### FAST-CHARGE State

In the FAST-CHARGE state, the charger operates in constant-current (CC) mode and regulates the charge current to the current set by  $R_{ISET}$ . Charging continues in CC mode until  $V_{BAT}$  reaches the charge termination voltage ( $V_{TERM}$ ), at which point the state-machine jumps to the TOP-OFF state. If  $V_{BAT}$  does not reach  $V_{TERM}$  before the total time out period expires then the state-machine will jump to the "EOC" state and will re-initiate a new charge cycle after 32ms "relax". See the *Current Limits* and *Charge Current Programming* sections for more information about setting the maximum charge current.

### TOP-OFF State

In the TOP-OFF state, the cell charges in constant-voltage (CV) mode. In CV mode operation, the charger regulates its output voltage to the 4.20V charge termination voltage, and the charge current is naturally reduced as the cell approaches full charge. Charging continues until the charge current drops to END-OF-CHARGE current threshold, at which point the state machine jumps to the END-OF-CHARGE (EOC) state.

If the state-machine does not jump out of the TOP-OFF state before the Total-Charge Time-out period expires, the state machine jumps to the EOC state and will re-initiate a new charge cycle if  $V_{BAT}$  falls below termination voltage 205mV (typ). For more information about the charge safety timers, see the *Charging Safety Times* section.

### END-OF-CHARGE (EOC) State

In the END-OF-CHARGE (EOC) state, the charger presents a high-impedance to the battery,

minimizing battery current drain and allowing the cell to "relax". The charger continues to monitor the cell voltage, and re-initiates a charging sequence if the cell voltage drops to 205mV (typ) below the charge termination voltage.

### SUSPEND State

The state-machine jumps to the SUSPEND state any time the battery is removed, and any time the input voltage either falls below the CHGIN UVLO threshold or exceeds the OVP threshold. Once none of these conditions are present, a new charge cycle initiates.

A charging cycle may also be suspended manually by setting the SUSPEND[ ] bit. In this case, initiate a new charging sequence by clearing SUSPEND[ ] to 0.

## State Machine Interrupts

The charger features the ability to generate interrupts when the charger state machine transitions, based upon the status of the CHG\_ bits. Set CHGEOCIN[ ] bit to 1 and CHGSTAT[ ] bit to 1 to generate an interrupt when the charger state machine goes into the END-OF-CHARGE (EOC) state. Set CHGEOCOUT[ ] bit to 1 and CHGSTAT[ ] bit to 1 to generate an interrupt when the charger state machine exits the EOC state.

CHGDAT[ ] indicates the status of the charger state machine. A value of 1 indicates that the charger state machine is in END-OF-CHARGE state, a value of 0 indicates the charger state machine is in other states.

When an interrupt is generated by the charger state machine, reading the CHGSTAT[ ] returns a value of 1. CHGSTAT[ ] is automatically cleared to 0 upon reading. When no interrupt is generated by the charger state machine, reading the CHGSTAT[ ] returns a value of 0.

For additional information about the charge cycle, CSTATE[0:1] may be read at any time via I<sup>2</sup>C to determine the current charging state.

**Table 11:**  
Charging Status Indication

| CSTATE[0] | CSTATE[1] | STATE MACHINE STATUS             |
|-----------|-----------|----------------------------------|
| 1         | 1         | PRECONDITION State               |
| 1         | 0         | FAST-CHARGE/<br>TOP-OFF State    |
| 0         | 1         | END-OF-CHARGE State              |
| 0         | 0         | SUSPEND/DISABLED/<br>FAULT State |

## Thermal Regulation

The charger features an internal thermal regulation loop that monitors die temperature and reduces charging current as needed to ensure that the die temperature does not exceed the thermal regulation threshold of 110°C. This feature protects against excessive junction temperature and makes the device more accommodating to aggressive thermal designs. Note, however, that attention to good thermal designs is required to achieve the fastest possible charge time by maximizing charge current.

## Charge Safety Timers

The charger features programmable charge safety timers which help ensure a safe charge by detecting potentially damaged cells. These timers are programmable via the PRETIMO[1:0] and TOTTIMO[1:0] bits, as shown in Table 12 and Table 13. Note that in order to account for reduced charge current resulting from DCCC operation, the charge time-out periods are extended proportionally to the reduction in charge current. As a result, the actual safety period may exceed the nominal timer period.

## Charger Timer Interrupts

The charger features the ability to generate interrupts based upon the status of the charge timers. Set the TIMRPRE[ ] bit to 1 and TIMRSTAT[ ] bit to 1 to generate an interrupt when the Precondition Timer expires. Set the TIMRTOT[ ] bit to 1 and TIMRSTAT[ ] bit to 1 to generate an interrupt when the Total-Charge Timer expires.

TIMRDAT[ ] indicates the status of the charge timers. A value of 1 indicates a precondition time-out or a total charge time-out occurs, a value of 0 indicates other cases.

When an interrupt is generated by the charge timers, reading the TIMRSTAT[ ] returns a value of 1. TIMRSTAT[ ] is automatically cleared to 0 upon reading. When no interrupt is generated by the charge timers, reading the TIMRSTAT[ ] returns a value of 0.

**Table 12:**

### PRECONDITION Safety Timer Setting

| PRETIMO[1] | PRETIMO[0] | PRECONDITION TIME-OUT PERIOD |
|------------|------------|------------------------------|
| 0          | 0          | 40 mins                      |
| 0          | 1          | 60 mins                      |
| 1          | 0          | 80 mins                      |
| 1          | 1          | Disabled                     |

**Table 13:**

### Total Safety Timer Setting

| TOTTIMO[1] | TOTTIMO[0] | TOTAL TIME-OUT PERIOD |
|------------|------------|-----------------------|
| 0          | 0          | 3 hrs                 |
| 0          | 1          | 4 hrs                 |
| 1          | 0          | 5 hrs                 |
| 1          | 1          | Disabled              |

## Charge Status Indicator

The charger provides a charge-status indicator output, nSTAT. nSTAT is an open-drain output which sinks current when the charger is in an active-charging state, and is high-Z otherwise. nSTAT features an internal 8mA current limit, and is capable of directly driving a LED without the need of a current-limiting resistor or other external circuitry. To drive an LED, simply connect the LED between nSTAT pin and an appropriate supply, such as VSYS. For a logic-level charge status indication, simply connect a resistor from nSTAT to an appropriate voltage supply.

**Table 14:**

### Charging Status Indication

| STATE             | nSTAT  |
|-------------------|--------|
| PRECONDITION      | Active |
| FAST-CHARGE       | Active |
| TOP-OFF           | Active |
| END-OF-CHARGE     | High-Z |
| SUSPEND           | High-Z |
| TEMPERATURE FAULT | High-Z |
| TIME-OUT-FAULT    | High-Z |

## Reverse-Current Protection

The charger includes internal reverse-current protection circuitry that eliminates the need for blocking diodes, reducing solution size and cost as well as dropout voltage relative to conventional battery chargers. When the voltage at CHGIN falls below  $V_{BAT}$ , the charger automatically reconfigures its power switch to minimize current drawn from the battery.

## Battery Temperature Monitoring

In a typical application, the TH pin is connected to the battery pack's thermistor input, as shown in

Figure 8. The charger continuously monitors the temperature of the battery pack by injecting a 102µA (typ) current into the thermistor (via the TH pin) and sensing the voltage at TH. The voltage at TH is continuously monitored, and charging is suspended if the voltage at TH exceeds either of the internal  $V_{THH}$  and  $V_{THL}$  thresholds of 0.5V and 2.51V, respectively.

The net resistance (from TH to GA) required to cross the thresholds are given by:

$$102\mu\text{A} \times R_{NOM} \times k_{HOT} = 0.5\text{V} \rightarrow R_{NOM} \times k_{HOT} \approx 5\text{k}\Omega$$

$$102\mu\text{A} \times R_{NOM} \times k_{COLD} = 2.51\text{V} \rightarrow R_{NOM} \times k_{COLD} \approx 25\text{k}\Omega$$

where  $R_{NOM}$  is the nominal thermistor resistance at room temperature, and  $k_{HOT}$  and  $k_{COLD}$  represent the ratios of the thermistor's resistance at the desired hot and cold thresholds, respectively, to the resistance at 25°C.

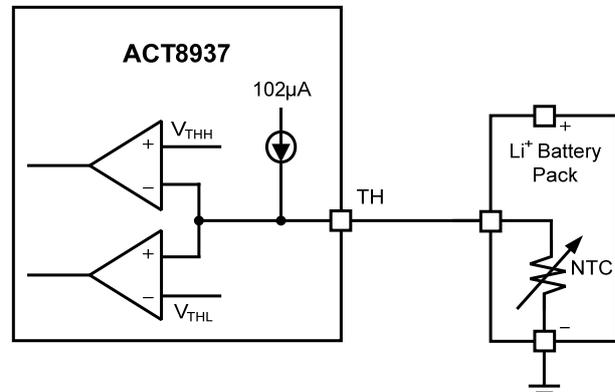
## Battery Temperature Interrupts

In order to ease detecting the status of the battery temperature, the charger features the ability to generate interrupts based upon the status of the battery temperature. Set the `TEMPOUT[ ]` bit to 1 and `TEMPSTAT[ ]` bit to 1 to generate an interrupt when battery temperature goes out of the valid temperature range. Set the `TEMPIN[ ]` bit to 1 and `TEMPSTAT[ ]` bit to 1 to generate an interrupt when battery temperature returns to the valid range.

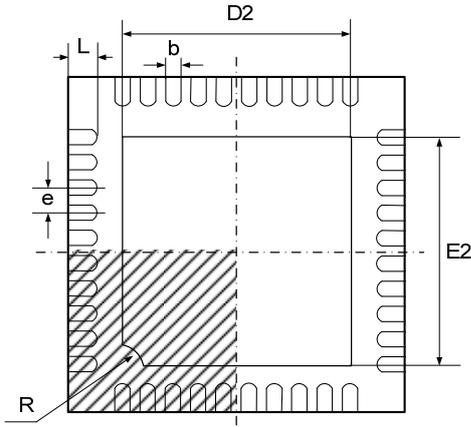
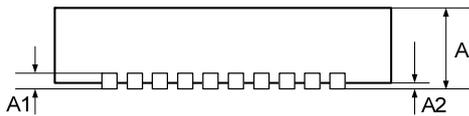
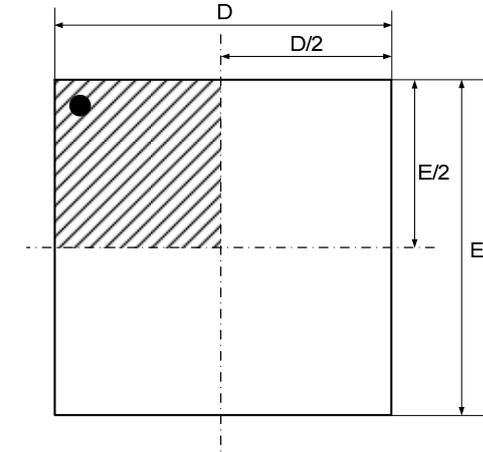
`TEMPDAT[ ]` indicates the status of the battery temperature. A value of 1 indicates the battery temperature is inside of the valid range, a value of 0 indicates the battery is outside of the valid range.

When an interrupt is generated by the battery temperature event, reading the `TEMPSTAT[ ]` returns a value of 1. `TEMPSTAT[ ]` is automatically cleared to 0 upon reading. When no interrupt is generated by the battery temperature event, reading the `TEMPSTAT[ ]` returns a value of 0.

**Figure 8:**  
**Simple Configuration**



## TQFN55-40 PACKAGE OUTLINE AND DIMENSIONS



| SYMBOL | DIMENSION IN MILLIMETERS |       | DIMENSION IN INCHES |       |
|--------|--------------------------|-------|---------------------|-------|
|        | MIN                      | MAX   | MIN                 | MAX   |
| A      | 0.700                    | 0.800 | 0.028               | 0.031 |
| A1     | 0.200 REF                |       | 0.008 REF           |       |
| A2     | 0.000                    | 0.050 | 0.000               | 0.002 |
| b      | 0.150                    | 0.250 | 0.006               | 0.010 |
| D      | 4.900                    | 5.100 | 0.193               | 0.201 |
| E      | 4.900                    | 5.100 | 0.193               | 0.201 |
| D2     | 3.450                    | 3.750 | 0.136               | 0.148 |
| E2     | 3.450                    | 3.750 | 0.136               | 0.148 |
| e      | 0.400 BSC                |       | 0.016 BSC           |       |
| L      | 0.300                    | 0.500 | 0.012               | 0.020 |
| R      | 0.300                    |       | 0.012               |       |

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