

# NXP4330D/Q

Application Processor

**Datasheet**

*Version 1.01*

## Section 1. **Product Overview**

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## 1.1 Introduction

NXP4330D/Q is a system-on-a-chip (SoC) based on the 32-bit RISC processor for tablets and cell-phones. Designed with the 28 nm low power process, features of NXP4330D/Q include:

- Cortex-A9 Dual/Quad core CPU
- Highest memory bandwidth
- Full HD display
- 1080p 60 frame video decoding and 1080p 30 frame encoding hardware
- 3D graphics hardware
- High-speed interfaces such as eMMC4.5 and USB 2.0

NXP4330D/Q uses the Cortex-A9 quad core, which is 50 % overall performance higher than Cortex-A8 core and its speed is 1.4GHz. It provides 6.4 GB/s memory bandwidth for heavy traffic operations such as 1080p video encoding and decoding, 3D graphics display and high resolution image signal processing with Full HD display. The application processor supports dynamic virtual address mapping, which helps software engineers to fully utilize the memory resources with ease.

NXP4330D/Q provides the best 3D graphics performance with wide range of APIs, such as OpenGL ES1.1, 2.0. Superior 3D performance fully supports Full HD display. The native dual display, in particular, supports Full HD resolution of a main LCD display and 1080p 60 frame HDTV display throughout HDMI, simultaneously. Separate post processing pipeline enables NXP4330D/Q to make a real display scenario.

### NOTE)

- NXP4330D : Cortex-A9 Dual Core CPU / NXP4330Q : Cortex-A9 Quad Core CPU
- NXP4330D and NXP4330Q are pin to pin compatible

## 1.2 Key Features

- 28nm, HKMG (High-K Metal Gate) Process Technology
- 513 pin FCBGA Package, 0.65mm Ball Pitch, 17x17mm Body size
- Cortex-A9 Dual/Quad Core CPU @ 1.4GHz
- High Performance 3D Graphic Accelerator
- Full-HD Multi Format Video Codec
- Supports various memory : x32 LPDDR2/3, LVDDR3(Low Voltage DDR3), DDR3 up to 800MHz
- Supports MLC/SLC NAND Flash with Hardwired ECC algorithm (4/8/12/16/24/40/60bit)
- Supports Dual Display up to 2048x1280, TFT-LCD, LVDS, HDMI 1.4a, MIPI-DSI output
- Supports 3ch ITUR.BT 656 Parallel Video Interface and MIPI-CSI
- Supports 10/100/1000M-bit Ethernet MAC
- Supports 3ch SD/MMC, 6ch UARTs, 32ch DMAs, 4ch Timer, Interrupt Controller, RTC
- Supports 3ch I2S, SPDIF Rx/Tx, 3ch I2C, 3ch SPI, 8ch 12bit ADC, 3ch PWM and GPIOs, 1ch PPM
- Supports MPEG-TS Serial/Parallel Interface and MPEG-TS HW Parser
- Supports 1ch USB 2.0 Host, 1ch USB 2.0 OTG, 1ch USB HSIC Host
- Supports Security functions (AES, DES/TDES, SHA-1, MD5 and PRNG) and Secure JTAG
- Supports various Power Mode (Normal, Sleep, Deep-Sleep, Stop)
- Supports various boot modes including NAND (with ECC detection and correction), SPI Flash/EEPROM, NOR, USB and UART

### 1.3 Block Diagram

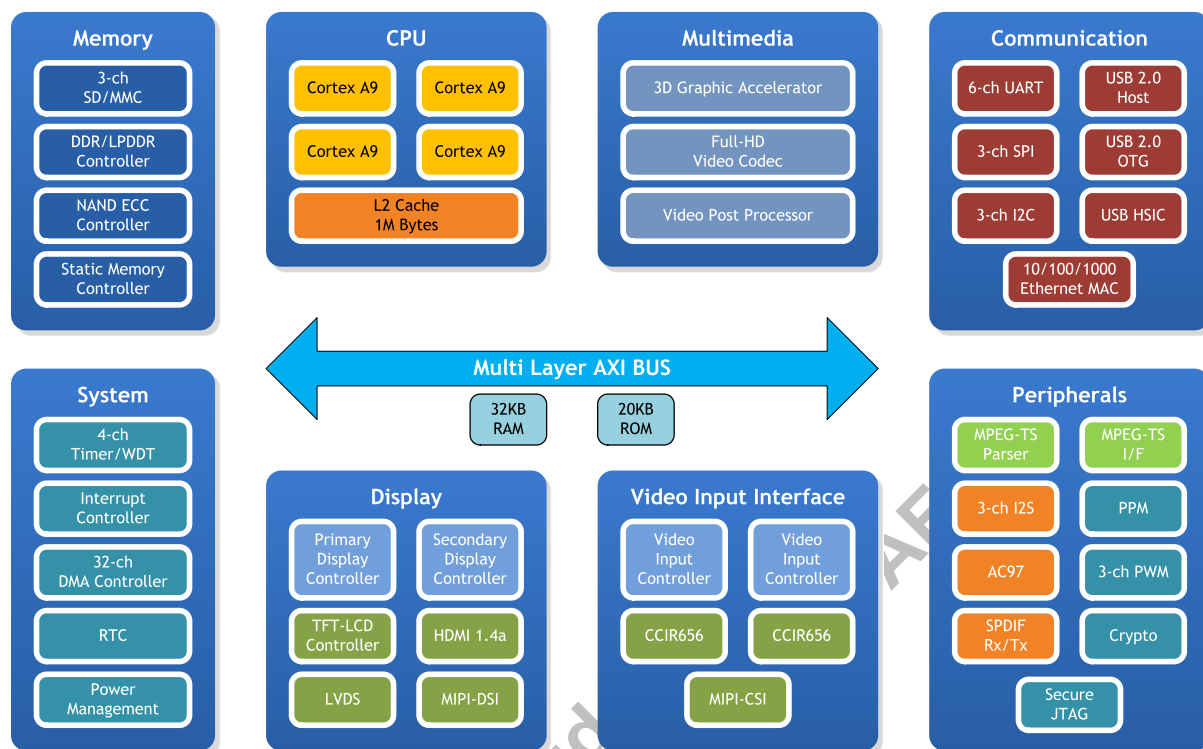


Figure 1-1. Block Diagram

## 1.4 Brief Functional Specification

### 1.4.1 CPU

- Cortex-A9 Dual/Quad Core @ 1.4GHz
- L1 Cache
  - 32Kbyte I-Cache, 32Kbyte D-Cache
- L2 Cache
  - 1Mbyte Shared Cache
- Co-Processor
  - VFP (Vector Floating Point Processor), Neon Processor

### 1.4.2 Clock &Power Management

- 4 Spread-Spectrum PLLs
- External Crystal : 24MHz(for PLL), 32.768Khz(for RTC)
- Supports for various power mode
  - Normal, Idle, Stop
  - Suspend to RAM (Sleep, Deep Sleep)

### 1.4.3 DMA

- 32-ch DMAs
- Operation Mode
  - Memory-to-Memory Transfer
  - Memory to IO Transfer, IO to Memory Transfer

### 1.4.4 Interrupt Controller

- Vectored Interrupt Controller
- Supports 64-ch Interrupt Sources
- Supports following features
  - fixed hardware interrupt priority levels
  - programmable interrupt priority levels
  - hardware interrupt priority level masking
  - programmable interrupt priority level masking
  - IRQ and FIQ generation
  - software interrupt generation
  - test registers
  - raw interrupt status
  - interrupt request status

### 1.4.5 Timer & Watchdog Timer

- 4-ch Timer with Watchdog Timer
- Normal interval timer mode with interrupt request
- Internal reset signal is activated when the timer count value reaches 0 (time-out)
- Level-triggered interrupt mechanism

### 1.4.6 RTC

- 32bit Counter
- Support Alarm Interrupt

### 1.4.7 Memory Controller

- System Memory Controller
  - Supports LPDDR2/LPDDR3/LVDDR3(Low Voltage DDR3)/DDR3 SDRAM up to 2Gbytes
  - Supports 1.2V ~ 1.5V power
  - Max Operation Frequency : 800MHz
  - Data Bus width : 32-bit
- Static Memory Controller
  - Multiplexed Address : up to 24-bit
  - SRAM, ROM and NAND Flash
  - Burst Read/Write
- NAND Flash Controller
  - Supports SLC/MLC NAND Flash
  - Supports MLC NAND Boot
  - Hardwired ECC Algorithm
    - 4/8/12/16/24/40/60-bit BCH Error Correction

### 1.4.8 GPIO Controller

- Various GPIO Interrupt Modes
  - Rising Edge, Falling Edge, High Level, Low Level Detection
- Individual Interrupt Generation

### 1.4.9 Ethernet MAC Controller

- Standard Compliance
  - IEEE 802.3az-2010, for Energy Efficient Ethernet (EEE)
  - RGMII specification version 2.6 from HP/Marvell
- MAC supports the following features
  - 10, 100, and 1000 Mbps data transfer rates with the following PHY interfaces:
    - RGMII interface to communicate with an external gigabit PHY
  - Full-duplex operation:

- IEEE 802.3x flow control automatic transmission of zero-quanta Pause frame on flow control input de-assertion
- Optional forwarding of received Pause frames to the user application
- Half-duplex operation:
  - CSMA/CD Protocol support
  - Flow control using backpressure support (based on implementation-specific white papers and UNH Ethernet Clause 4 MAC Test Suite - Annex D)
  - Frame bursting and frame extension in 1000 Mbps half-duplex operation
- Preamble and start of frame data (SFD) insertion in Transmit path
- Preamble and SFD deletion in the Receive path
- Automatic CRC and pad generation controllable on a per-frame basis
- Automatic Pad and CRC Stripping options for receive frames
- Flexible address filtering modes, such as:
  - Up to 31 additional 48-bit perfect (DA) address filters with masks for each byte
  - Up to 96 additional 48-bit perfect (DA) address filters that can be selected in blocks of 32 and 64 registers
  - Up to 31 48-bit SA address comparison check with masks for each byte
  - 64-bit, 128-bit, or 256-bit Hash filter (optional) for multicast and unicast (DA) addresses
  - Option to pass all multicast addressed frames
  - Promiscuous mode to pass all frames without any filtering for network monitoring
  - Pass all incoming packets (as per filter) with a status report
- Programmable frame length to support Standard or Jumbo Ethernet frames with up to 16 KB of size
- Programmable Interframe Gap (IFG) (40-96 bit times in steps of 8)
- Option to transmit frames with reduced preamble size
- Separate 32-bit status for transmit and receive packets
- IEEE 802.1Q VLAN tag detection for reception frames
- Additional frame filtering:
  - VLAN tag-based: Perfect match and Hash-based (optional) filtering
  - Layer 3 and Layer 4-based: TCP or UDP over IPv4 or IPv6
- Separate transmission, reception, and control interfaces to the application
- MDIO master interface (optional) for PHY device configuration and management
- Standard IEEE 802.3az-2010 for Energy Efficient Ethernet
- CRC replacement, Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted frames with per-frame control
- Programmable watchdog timeout limit in the receive path

#### 1.4.10 SD/MMC Controller

- 3 Independent SD/MMC Controller and Ports
- Secure Digital Memory (SD mem- version 3.0)
- Secure Digital I/O (SDIO - version 3.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA - version 1.1)



- Multimedia Cards (MMC - version 4.41, eMMC 4.5)
- Supports following features of MMC4.41
- Support following features of eMMC4.5
- Support clock speed up to 50 MHz
- Support PIO and DMA mode data transfer
- Support 1/4-bit data bus widths
  - Overlay SPI signals to same GIOs from SSP/SPI controller

#### 1.4.11 PPM

- Pulse Period Measurement for IR remote receiver

#### 1.4.12 PWM

- 3-ch PWM Controller
- Five 32-bit Timers
- Two 8-bit Clock Prescalers providing first level of division for the PCLK, Five Clock Dividers and Multiplexers providing second level of division for the Prescaler clock and Two External Clocks
- Programmable Clock Select Logic for individual PWM Channels
- Four Independent PWM Channels with Programmable Duty Control and Polarity
- Static Configuration: PWM is stopped
- Dynamic Configuration: PWM is running
- Supports Auto-Reload Mode and One-Shot Pulse Mode
- Supports for two external inputs to start PWM
- Dead Zone Generator on two PWM Outputs
- Supports DMA Transfers
- Optional Pulse or Level Interrupt Generation
- The PWM has two operation modes:
  - Auto-Reload Mode
    - Continuous PWM pulses are generated based on programmed duty cycle and polarity
  - One-Shot Pulse Mode
    - Only one PWM pulse is generated based on programmed duty cycle and polarity

#### 1.4.13 ADC

- 8-ch analog input port
- Supports following features
  - Resolution: 12-bit
  - Conversion rate : 1MSPS
  - Power consumption
    - 1.0 mW ( Fs = 1MSPS ) @ Normal operation mode Typ.

- 0.005 mW @ Power down mode Typ.
- Input range: 0 ~ AVDD18
- Input frequency: up to 100kHz
- Digital output: CMOS Level (0 ~ AVDD10)

#### 1.4.14 I2C

- 3-ch I2C bus controller
- Each device connected to the bus is software addressable by a unique address and simple master/slave relationships exist at all times; master can operate as master-transmitter or as master-receiver
- Serial, 8-bit oriented, bi-directional data transfers can be made at up to 100kbit/s in the Standard-mode, up to 400kbit/s in the Fast-mode
- The number of ICs that can be connected to the same bus is limited only by a maximum bus capacitance of 400pF
- Repeated START and early termination function are not support
- High speed mode, combined format, 10bit address are not supported

#### 1.4.15 SPI/SSP

- 3-ch SPI Controller
- Master or slave operation.
- Programmable clock bit rate and prescale.
- Separate transmit and receive first-in, first-out memory buffers, 16 bits wide, 8 locations deep.
- Programmable choice of interface operation, SPI, Microwire, or TI synchronous serial.
- Programmable data frame size from 4 to 16 bits.
- Independent masking of transmit FIFO, receive FIFO, and receive overrun interrupts.
- Internal loopback test mode available.
- Support for Direct Memory Access (DMA).

#### 1.4.16 MPEG-TS

- Supports Serial & Parallel MPEG-TS Interface
- Supports Hardwired MPEG2-TS parser for Set-top and IPTV

#### 1.4.17 UART& ISO7816 Sim Card Interface

- 6-ch UART controller
- Programmable use of UART or IrDA SIR input/output.
- Separate 32×8 transmit and 32×12 receive First-In, First-Out (FIFO) memory buffers to reduce CPU interrupts.
- Programmable FIFO disabling for 1-byte depth.

- Programmable baud rate generator. This enables division of the reference clock by  $(1 \times 16)$  to  $(65535 \times 16)$  and generates an internal  $\times 16$  clock. The divisor can be a fractional number enabling you to use any clock with a frequency  $> 3.6864\text{MHz}$  as the reference clock.
- Standard asynchronous communication bits (start, stop and parity). These are added prior to transmission and removed on reception.
- Independent masking of transmit FIFO, receive FIFO, receive timeout, modem status, and error condition interrupts.
- Support for Direct Memory Access (DMA).
- False start bit detection.
- Line break generation and detection.
- Support of the modem control functions CTS, DCD, DSR, RTS, DTR, and RI.
- Programmable hardware flow control.
- Fully-programmable serial interface characteristics:
  - data can be 5, 6, 7, or 8 bits
  - even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
  - baud rate generation, dc up to  $\text{UARTCLK}/16$
- IrDA SIR ENDEC block providing:
  - programmable use of IrDA SIR or UART input/output
  - support of IrDA SIR ENDEC functions for data rates up to 115200 bps half-duplex
  - support of normal 3/16 and low-power (1.41-2.23 $\mu\text{s}$ ) bit durations
  - programmable division of the  $\text{UARTCLK}$  reference clock to generate the appropriate bit duration for low-power IrDA mode.
- Identification registers that uniquely identify the UART. These can be used by an operating system to automatically configure itself.

#### 1.4.18 USB

- 1-ch USB 2.0 Host and 1-ch USB2.0 HSIC Host
  - fully compliant with the Universal Serial Bus Specification, Revision 1.1, Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 2.0, and the openHCI: Open Host Controller Interface Specification for USB, Release 1.0a. The controller supports high-speed, 480-Mbps transfers (40 times faster than USB 1.1 full-speed mode) using an EHCI Host Controller, as well as full and low speeds through one or more integrated OHCI Host Controllers.
  - At the USB 2.0 physical interface, the controller provides the following:
    - UTMI: UTMI+ Level 3, Revision 1.0
    - High-Speed Inter-Chip (HSIC), Version 1.0
  - Supports ping and split transactions
  - UTMI/UTMI+ PHY interface clock supports 30-MHz operation for a 16-bit interface or 60-MHz operation for an 8-bit interface
  - Heterogeneous selection of UTMI+ or HSIC interfaces per port using strap pins. In Heterogeneous mode, only the 8-bit interface (60 MHz) is supported.
- 1-ch USB 2.0 OTG Controller

- supports both device and host functions and complies fully with the On-The-Go Supplement to the USB 2.0 Specification, Revision 1.3a and Revision 2.0. It can also be configured as a host-only or device-only controller, fully compliant with the USB 2.0 Specification.
- Complies with the On-The-Go Supplement to the USB 2.0 Specification (Revision 1.3)
- Complies with the On-The-Go Supplement to the USB 2.0 Specification (Revision 2.0)
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- Support for the following speeds:
  - High-Speed (HS, 480-Mbps),
  - Full-Speed (FS, 12-Mbps) and
  - Low-Speed (LS, 1.5-Mbps) modes
- Multiple options available for low power operations
- Multiple DMA/non DMA mode access support on the application side
- Multiple Interface support on the MAC-Phy
- Supports 16 bidirectional endpoints, including control endpoint 0.
- Supports Session Request Protocol (SRP)
- Supports Host Negotiation Protocol (HNP)
- Supports up to 16 host channels. In Host mode, when the number of device endpoints to be supported is more than the number of host channels, software can reprogram the channels to support up to 127 devices, each having 32 endpoints (IN + OUT), for a maximum of 4,064 endpoints.
- Includes automatic ping capabilities

#### 1.4.19 I2S

- 3-ch I2S Controller for 5.1ch Audio output
- 16bit/24bit Master & Slave Mode
- Supports various interface mode
  - I2S, Left-justified, Right-Justified, DSP mode
- Supports TDM mode for Digital MIC interface
- Supports SPDIF Rx/Tx

#### 1.4.20 AC97

- 1-Ch AC97
- Independent channels for stereo PCM In, stereo PCM Out, mono MIC In
- DMA-based operation and interrupt based operation
- All of the channels support only 16-bit samples
- Variable sampling rate AC97 Codec interface (48 kHz and below)
- 16-bit, 16 entry FIFOs per channel
- Only primary Codec support

#### 1.4.21 SPDIF Tx, Rx

- SPDIF Tx

- Supports linear PCM up to 24-bit per sample
- Supports Non-linear PCM formats such as AC3, MPEG1 and MPEG2
- 2x24-bit buffers which is alternately filled with data
- SPDIF Rx
  - Serial, unidirectional, self-clocking interface
  - Single wire-single signal interface
  - Easy to work because it is polarity independent

#### 1.4.22 PDM

- Supports receiving 2 channel audio data with 1 data pin
- 1 output clock pin
- 2 data pins ( total 4 channel accepts available )
- Fixed output clock frequency
- Supports select of the timing of data capture
- Supports DMA interface
- Supports a user configuration of Coefficient. (Butterworth Low-pass Filter)

#### 1.4.23 Display Controller

- Supports Dual Display
- Supports 3 Layers, Gamma Correction and Color Control (Brightness, Contrast, Hue and Saturation)
- Supports various Pixel Format
  - RGB/BGR 444,555,565,888 with/without Alpha channel
- Resolution
  - Up to 2048x1280 @60hz
- Supports various LCD
  - I80 Interface, RGB, Serial RGB, LVDS output
  - Supports MIPI-DSI 4 data lanes
- HDMI Interface
  - HDMI 1.4a, HDCP 1.4 Complaint
  - Supports Video format:
    - 480p @59.94Hz/60Hz, 576p@50Hz
    - 720p @50Hz/59.94Hz/60Hz
    - 1080p @50Hz/59.94Hz/60Hz
    - Primary 3D Video Formats
    - Other various formats up to 148 MHz Pixel Clock
  - Supports Color Format : 4:4:4 RGB/YCbCr , 4:2:2 YCbCr
  - Pixel Repetition : Up to x4
  - Supports Bit Per Color : 8bit, 10bit ,12bit (Note: 16bit not supported)
  - Dedicated block for CEC function
  - Supports : Linear-PCM, Non-linear PCM and high-bitrate audio formats (Audio Sample packets and HBR)

- packets for audio transmission)
- Integrated HDCP Encryption Engine for Video/Audio content protection (Authentication procedure are controlled by S/W, not by H/W)
- A dedicated CEC module (Separated for power/clock domain separation)
- SPDIF Interface and I2S interface for Audio Input
- Supports level-triggered Interrupt and SFR for HPD
- Supports AES KEY Decryption Function for external HDCP Key management
- LVDS Interface
  - Output clock range: 30M to 90MHz
  - 35:7 data channel compression up to 630Mbps on each LVDS channel
  - Power down mode
  - Up to 393.75Mbytes/sec bandwidth
  - Falling clock edge data strobe
  - Narrow bus reduces cable size and cost
  - PLL requires no external component
  - 6 LVDS output channels (5 data channels, 1 clock channel)
- MIPI-DSI
  - Complies to MIPI DSI Standard Specification V1.01r11
    - Maximum resolution ranges up to WUXGA (1920x1200)
    - Supports 1, 2, 3, or 4 data lanes
    - Supports pixel format: 16bpp, 18bpp packed, 18bpp loosely packed (3 byte format), and 24bpp
  - Interfaces
    - Complies with Protocol-to-PHY Interface (PPI) in 1.5Gbps MIPI D-PHY
    - Supports RGB Interface for Video Image Input from display controller
    - Supports I80 Interface for Command Mode Image input from display controller
    - Supports PMS control interface for PLL to configure byte clock frequency
    - Supports Prescaler to generate escape clock from byte clock

#### 1.4.24 Video Post Processor

- 3D De-interlace Controller
- Fine Scalar for video : Poly-phase filter

#### 1.4.25 Video Input Processor

- Max. 8192x8192 resolution support
- Supports x2 8bit BT656, 601 format
- Supports MIPI-CSI
  - General Features
    - Support primary and secondary Image format
      - YUV420, YUV420(Legacy), YUV420(CSPS), YUV422 of 8-bits and 10-bits
      - RGB565, RGB666, RGB888

- RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
- Compressed format : 10-6-10, 10-7-10, 10-8-10
- All of User defined Byte-based Data packet
- Support embedded byte-based non Image data packet and generic short packets.
- Compatible to PPI(Protocol-to-PHY Interface) in MIPI D-PHY Specification
- Support 4 channel virtual channel or data interleave
- Standard Compliance
  - Compliant to MIPI CSI2 Standard Specification V1.01r06
  - D-phy standard specification V1.0

### 1.4.26 Multi Format MPEG codec

- Decoder
  - H.264
    - BP, MP, HP profile, Level 4.2 up to 1920x1080, 50Mbps
  - MPEG4 ASP
    - Advanced Simple Profile up to 1920x1080, 40Mbps
  - H.263
    - Profile3 up to 1920x1080, 20Mbps
  - VC-1
    - SP/MP/AP profile, Level 3 up to 1920x1080, 2048x1024, 45Mbps
  - MPEG-1/2
    - Main Profile, High Level up to 1920x1080, 80Mbps
  - VP8
    - up to 1920x1080, 20Mbps
  - Theora
    - up to 1280x720, 20Mbps
  - AVS
    - Jizhun Profile, Level 6.2 up to 1920x1080, 40Mbps
  - RV8/9/10
    - up to 1920x1080, 40Mbps
  - MJPEG
    - Baseline profile up to 8192x8192
- Encoder
  - H.264
    - Baseline Profile, Level 4.0 up to 1080p, 20Mbps
  - MPEG4
    - Simple Profile, Level 5.6 up to 1080p, 20Mbps
  - H.263
    - Profile3, Level 70 up to 1080p, 20Mbps
  - MJPEG

- Baseline Profile up to 8192x8192

### 1.4.27 3D Graphic Controller

- Supports OpenGL|ES 1.0 and 2.0
- Supports OpenVG 1.1
- GPU is a hardware accelerator for 2D and 3D graphics systems.
- The GPU consists of:
  - one to four Pixel Processors (PPs)
  - a Geometry Processor (GP)
  - a Level 2 Cache Controller (L2)
  - a Memory Management Unit (MMU) for each GP and PP included in the GPU
  - a Power Management Unit (PMU).
- Pixel processor features
  - each pixel processor used processes a different tile, enabling a faster turnaround
  - programmable fragment shader
  - alpha blending
  - complete non-power-of-2 texture support
  - cube mapping
  - fast dynamic branching
  - fast trigonometric functions, including arctangent
  - full floating-point arithmetic
  - framebuffer blend with destination Alpha
  - indexable texture samplers
  - line, quad, triangle and point sprites
  - no limit on program length
  - perspective correct texturing
  - point sampling, bilinear, and trilinear filtering
  - programmable mipmap level-of-detail biasing and replacement
  - stencil buffering, 8-bit
  - two-sided stencil
  - unlimited dependent texture reads
  - 4-level hierarchical Z and stencil operations
  - Up to 512 times Full Scene Anti-Aliasing (FSAA). 4x multisampling times 128xsupersampling
  - 4-bit per texel compressed texture format.
- Geometry processor features
  - programmable vertex shader
  - flexible input and output formats
  - autonomous operation tile list generation
  - indexed and non-indexed geometry input
  - primitive constructions with points, lines, triangles and quads.
- Level 2 cache controller features
  - sizes of 32KB



- 4-way set-associative
- supports up to 32 outstanding AXI transactions
- implements a standard pseudo-LRU algorithm
- cache line and line fill burst size is 64 bytes
- supports eight to 64bytes uncached read bursts and write bursts
- 128-bit interface to memory sub-system
- support for hit-under-miss and miss-under-miss with the only limitation of AXI ordering rules.
- MMU features
  - accesses control registers through the bus infrastructure to configure the memory system.
  - each processor has its own MMU to control and translate memory accesses that the GPU initiates.
- PMU features
  - programmable power management
  - powers up and down each GP, PP and Level 2 cache controller separately
  - controls the clock, isolation and power of each device
  - provides an interrupt when all requested devices are powered up

#### 1.4.28 Security IP

- On-chip secure boot ROM/RAM
- Hardware Crypto Accelerator
  - DES/TDES, AES, SHA-1, MD5 and PRNG
- Supports Secure JTAG

#### 1.4.29 Unique Chip ID

- Supports 128-bit Unique Chip ID register

#### 1.4.30 Operating Conditions

- Operation Voltage
  - Core : 1.0V
  - CPU : 1.0V ~ 1.3V
  - DDR Memory : 1.2~1.5V
  - I/O : 3.3V
- Operation Temperature
  - T.B.D

#### 1.4.31 Package

- 513 pin FCBGA
- Ball Pitch: 0.65 mm
- Body Size : 17x17 mm